BACHELOR THESIS

Electrical engineering, electronics

College of Engineering and Architecture of Fribourg

member of University of Applied Sciences of Western Switzerland

---

Sensor Module Studies

LARGE HADRON COLLIDER, ATLAS EXPERIMENT, SILICON TRACKER

Student :
Michaël DEFFERRARD

Supervisors :
Carl H. HABER
Sergio DÍEZ CORNELL

Advisers :
Marco MAZZA
Ottar JOHNSEN

Expert :
Luciano SBAIZ

Proposed by Lawrence Berkeley National Laboratory
University of California, Berkeley

August 14, 2012

This page is intentionally left blank.

Abstract

This thesis is about the studies of silicon sensors arrays for the ATLAS detector upgrade. The main goal of this work is to assemble and test the US Stavelet. This project is decomposed into three parts : the Stavelet assembly, the test systems and the electrical measurements. This work involves a global understanding of the subject, precision assembly, metrology measurements, the installation and characterization of a test setup, the development of a LabVIEW based software, noise measurements and analysis.

Résumé

Cette thèse a pour sujet l'étude d'ensembles de capteurs silicium pour la mise à jour du détecteur ATLAS. Le but principal du travail est d'assembler et tester l'"US Stavelet". Ce projet est décomposé en trois parties : l'assemblage de la "Stavelet", les systèmes de tests et les mesures électriques. Ce travail demande un compréhension globale du sujet, de l'assemblage de précision, des mesures métrologiques, l'installation et la caractérisation d'une installation de test, le dévelopement d'un logiciel basé sur LabVIEW, des mesures et analyses de bruit.

Zusammenfassung

Diese Arbeit beschäftigt sich mit den Studien der Gesamtheit von den Silizium Sensoren für die Aktualisierung des ATLAS-Detektors. Das Hauptziel dieser Arbeit ist die ÜS Staveletßusammen zu fügen und zu testen. Dieses Projekt ist in drei Teile zerlegt : die SStaveletSZusammensetzung, die Testsysteme und die elektrischen Messungen. Diese Arbeit beinhaltet eine globale Verständnis des Themas, Präzision Zusammensetzung, metrologischen Messungen, die Installation und Charakterisierung eines test setup", die Entwicklung einer LabVIEW-basierten Software, Lärmmessungen und deren Analysen.

Acknowledgements

A special thank goes to Carl H. Haber, my supervisor at the Lawrence Berkeley National Laboratory. I'm grateful for all the inputs and explanations from his profound knowledge about silicon detectors and the whole ATLAS experiment. I would also thank Sergio Díez Cornell, post-doctoral researcher at Berkeley Lab. He supported me during the project and gave me explanations and references. He also took the time to read parts of my thesis and to point out some misunderstandings. I take profit from his knowledge about particle physics and the ATLAS experiment. Thanks to Rhonda Witharm, our technician, for all her advices and her patience.

Thanks to Marco Mazza and Ottar Johnsen, professors at the College of Engineering and Architecture of Fribourg, for their support, encouragement and visit.

Thanks to Niklaus Lehman, who motivated me to do my bachelor thesis at LBNL, and for his thesis, a good introduction to the subject.

Thanks to Peter W. Phillips (Rutherford Appleton Laboratory, Chilton, UK) and Matt Warren (University College London, London, UK) for all their advices about test software and firmware.

I would also thanks all the other people who helped me, gave me helpful advices or provided me with references during this project.

Contents

List of Figures

List of Tables

Revision history

Object of revision	Date	Rev.
Creation of this document	05/30/2012	1.0
SCT HV card description	06/01/2012	1.1
Introduction	06/03/2012	1.2
Power supplies controller : requirements and LabVIEW program	06/06/2012	1.3
Single module test procedure	06/08/2012	1.4
Module, Core and Stavelet description	06/14/2012	1.5
Comparison of noise between Module and Stavelet test setups	06/19/2012	1.6
Reviewing of section 5.2 : the results will be presented to all involved groups around the world at CERN Module building meeting on June 27.	06/25/2012	1.7
SCT HV controllers user manual : part 1 and 2	06/27/2012	1.8
Title page	07/02/2012	1.9
Core metrological measurements	07/04/2012	1.10
SCT HV controllers	07/06/2012	1.11
Conclusion	07/09/2012	1.12
Abstract and introduction upgrade	07/10/2012	1.13
Spelling correction and general revision. First version sent back to Fribourg.	07/12/2012	1.14
Noise measurements theory	08/10/2012	2.0
Readout electronics	08/08/2012	2.1
Complete test setups noise measurements	07/17/2012	2.2
Stavelet Core raw metrological measurements	07/20/2012	2.3
Module test setup upgraded	07/23/2012	2.4
Create glossary and acronyms	08/05/2012	2.5
Rearrange and write the chapter about Stavelet	08/05/2012	2.6
Stavelet assembly	08/09/2012	2.7
Chapter 4 upgraded	08/11/2012	2.8
Module and Stavelet noise analysis	08/11/2012	2.9
Chapter 3 revised	08/12/2012	2.10
Chapter 2 upgraded	08/12/2012	2.11
Introduction and conclusion updated	08/13/2012	2.12
Abstract in German and French	08/13/2012	2.13
Spelling correction and general revision. Final version.	08/14/2012	2.14

Glossary

Core The Stavelet Core is a thermo-mechanical assembly that holds and cools down the Modules. It also transmit electrical power and signals to and from them. 12, 17, 18, 20, 21, 25, 34, 44, 46, 54

ENC Equivalent Noise Charge, the number of electrons one would have to collect from a silicon sensor in order to create a signal equivalent to the noise of this sensor. 42, 44

Hybrid A flex Hybrid hosts the readout ASICs, the ABCNs. It is glued on the silicon sensor and is part of a Module. 15–17, 20, 28, 30–32, 34, 36, 44–47

LabVIEW (short for Laboratory Virtual Instrumentation Engineering Workbench) is a system design platform and development environment for a visual programming language from National Instruments. 34, 36–38, 53

Module A Module is a silicon strip sensor with integrated readout and control electronics. 9, 12, 15–17, 19, 25, 26, 32–36, 39–41, 44–47, 49, 51–54

ROOT The ROOT system, developed by CERN, provides a set of object oriented frameworks with all the functionality needed to handle and analyse large amounts of data in a very efficient way. Included are histograming methods, curve fitting, function evaluation, minimization, graphics and visualization classes to allow the easy setup of an analysis system that can query and process the data interactively or in batch mode. 41

SCTDAQ SemiConductor Tracker Data AcQuisition, a ROOT based software providing support for Module testing. 32, 41–44, 51, 55

Silicon tracker Silicon tracker, the upgraded ATLAS inner detector. 11, 12

Stavelet A Stavelet is a prototype and a shortened version of a Stave with four Modules per side. 9, 12, 14, 17–21, 31, 33–37, 40, 44–47, 49–53

subVI A LabVIEW subVI is equivalent to a function, subroutine, or method in other programming languages. It is useful for encapsulating code that will be reused multiple time. A subVI is also used to develop hierarchical programs. 37–39

VMEbus is a computer bus standard, originally developed for the Motorola 68000 line of CPUs, but later widely used for many applications and standardized by the IEC as ANSI/IEEE 1014-1987. 36, 37

Acronyms

ABCN ATLAS Binary Chip Next. 15–17, 24, 32, 34, 41, 42, 45

ALICE A Large Ion Collider Experiment. 10

ASIC Application Specific Integrated Circuit. 15, 16

ATLAS A Toroidal LHC ApparatuS. 9–12, 16, 34, 36, 53, 54

BCC Buffer Control Chip. 15, 16, 18, 31, 32, 35

CAD Computer-Aided Design. 25, 26

CERN European Organization for Nuclear Research. 10

CMOS Complementary metal-oxide-semiconductor. 16

CMS Compact Muon Solenoid. 10

CNC Computer Numerical Control. 26

DAQ Data AcQuisition. 11, 34

EIA-FR College of Engineering and Architecture of Fribourg. 9

EOS End Of Stave. 12, 17, 18, 31, 32, 35

FPGA Field Programmable Gate Array. 34, 35

HCC Hybrid Control Chip. 16

HES-SO University of Applied Sciences of Western Switzerland. 9

HL-LHC High Luminosity LHC. 10, 11

HSIO High Speed Input Output. 12, 32, 34–36, 41, 46–48, 51

HV High Voltage (silicon sensor bias voltage). 12, 18, 28, 30–32, 36, 39, 40, 50, 53

IBL Insertable B-Layer. 11

ID Inner Detector. 10, 11

IO Input/Output. 32, 34

LBNL Lawrence Berkeley National Laboratory. 9, 12, 19, 20, 53, 54

LED Light-Emitting Diode. 39

LHC Large Hadron Collider. 10

LHCb Large Hadron Collider beauty. 10

LV Low Voltage (supply the electronic on the Hybrid). 18, 32, 36, 49, 50

LVDS Low Voltage Differential Signaling. 12

NI-VISA National Instrument Virtual Instrument Software Architecture. 37

PS Power Supply. 12, 18, 32, 36, 39, 49, 50

SCT SemiConductor Tracker. 10

SCT HV SemiConductor Tracker High Voltage. 32, 36, 38, 53

SNR Signal-to-Noise Ratio. 14

ToT Time over Threshold. 15

TRT Transition Radiation Tracker. 10

VI Virtual Instrument. 38

1 Introduction

This thesis, conducted at Lawrence Berkeley National Laboratory (LBNL), is the conclusion of my bachelor studies in electrical engineering at the College of Engineering and Architecture of Fribourg (EIA-FR), member of the University of Applied Sciences of Western Switzerland (HES-SO).

This work is about the studies of silicon sensors arrays that will be part of the upgraded version of the A Toroidal LHC ApparatuS (ATLAS) detector. The main goal of this work is to build and test the US Stavelet. To achieve this goal, we use some existing tools and test setup but we also need to create some new tools and setups. The development of these tools is part of this thesis too.

Last year, Niklaus Lehmann, another student from EIA-FR, worked on the Modules, Stavelet sub-assemblies. [Leh11] This thesis is a continuation of his work, by putting Modules together to assemble a Stavelet and test them.

We will first introduce the subject, starting from the accelerator down to the Stavelet. An introduced reader can skip this chapter. We will then go trough the three parts of this project. First the Stavelet assembly, describing progressively its sub-components, the developed and used mounting tools, the metrological measurements. Then the used and installed Stavelet test systems. Finally the electrical measurements, including analysis, both on single Modules and on the Stavelet. The annexes contain the test procedures, the developed software user manual, the raw metrological measurements.

2 LHC and ATLAS, briefly

The Large Hadron Collider (LHC) is the largest and highest-energy particle collider actually in service. It was built by the European Organization for Nuclear Research (CERN) from 1998 to 2008, with the aim of allowing physicists to test the predictions of different theory of particle physics and high-energy physics. It contains four detectors each designed for specific kinds of exploration : ATLAS, Compact Muon Solenoid (CMS), A Large Ion Collider Experiment (ALICE) and Large Hadron Collider beauty (LHCb). The LHC upgrade to the High Luminosity LHC (HL-LHC), scheduled for 2022, will increase the machine luminosity[1] by a factor of five to ten.

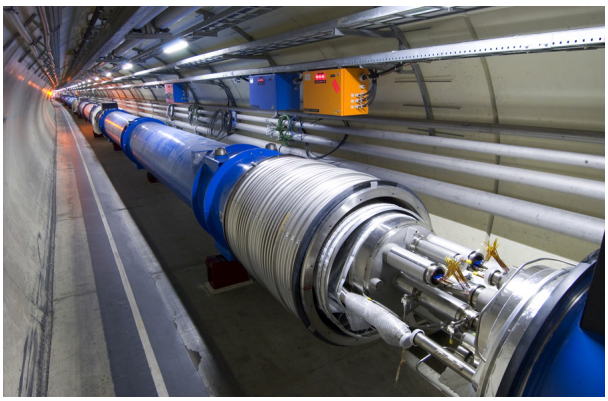
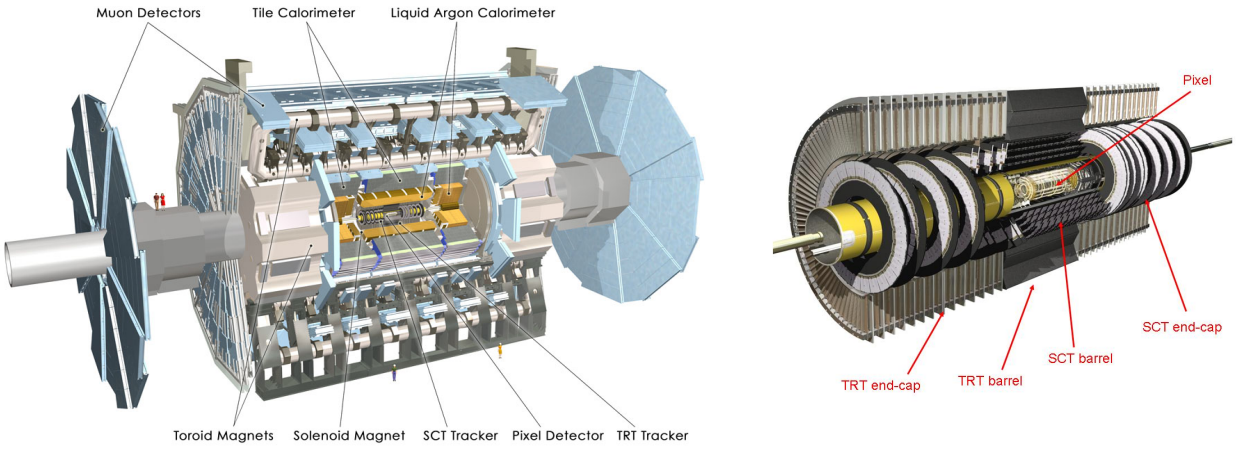


Figure 1: Tunnel of the Large Hadron Collider

ATLAS is one of two larger general purpose magnetic spectrometers at the LHC. It is composed of three sub-detectors : the Inner Detector (ID), the calorimeters and the muon chambers. The ID is itself composed by three trackers : the Transition Radiation Tracker (TRT), the SemiConductor Tracker (SCT) and the pixel. The current detector is shown on figures 2(a) and 2(b).



(a) Entire detector

(b) Inner detector

Figure 2: Current ATLAS detector

[1] In scattering theory and accelerator physics, luminosity is the number of particles per unit area per unit time times the opacity of the target, usually expressed in either $cm^{-2}s^{-1}$ or $b^{-1}s^{-1}$. The integrated luminosity is the integral of the luminosity with respect to time. The luminosity is an important value to characterize the performance of an accelerator.

Three upgrade steps are scheduled for the ATLAS experiment in the following years : Phase-0, Phase-I and Phase-II. [MC12] Phase-0 is mostly focused on the innermost pixel detector, in particular the insertion of an additional pixel layer : the Insertable B-Layer (IBL) which enhances vertex tracking. Phase-I is mainly upgrades to trigger and Data AcQuisition (DAQ). Phase-II, also called ATLAS Upgrade, is the one needed for the HL-LHC, and will require the ID to be replaced by a new, all Silicon tracker, with higher granularity, faster readout electronics and higher radiation tolerance. Figure 3 shows a possible layout of the Silicon tracker, composed of the pixel, a barrel (short strips and long strips) and two end-caps.

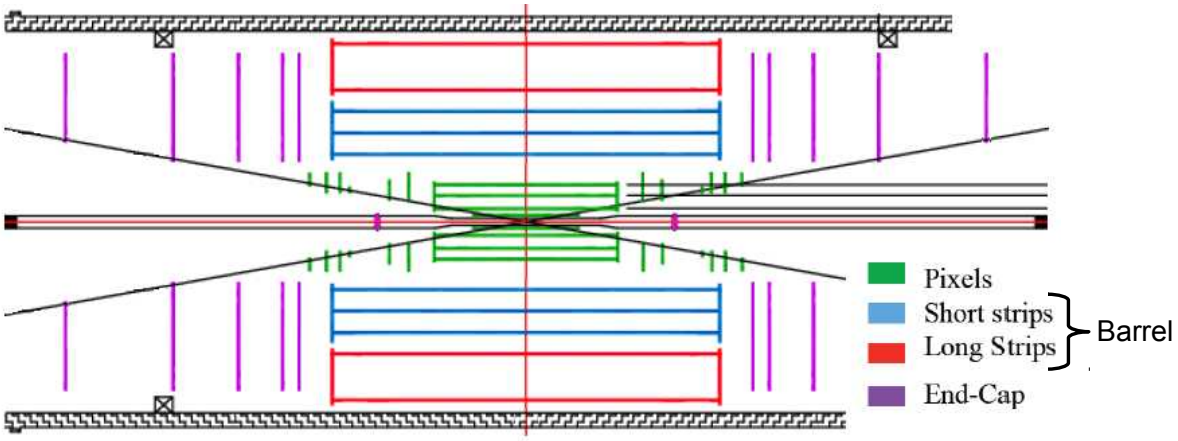


Figure 3: Silicon tracker layout after Phase-II upgrade [SDC11]

Figure 4 shows the strips barrel and end-cap composition.

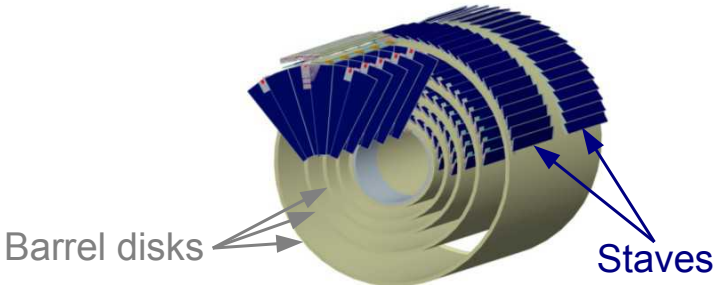


Figure 4: Strips silicon tracker : barrel and end-cap [SDC11]

The baseline solution for the strips barrel is the Stave concept, shown on figure 5, in which a number of single sided silicon strip detector modules are glued directly to each side of a composite support structure with carbon fibre skins.

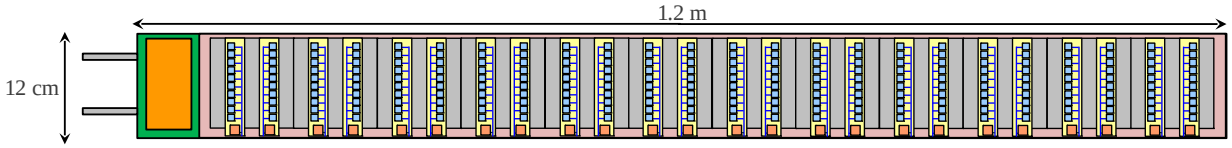


Figure 5: Stave [SDC11]

3 Stavelet

A Stave is an assembly of silicon strip sensors with integrated control electronics, so called Modules. These are hold and cooled down by a thermo-mechanical assembly, the Core. The latest layout of the Silicon tracker has thirteen Modules per side. A Stavelet is a shortened Stave prototype with four Modules per side.

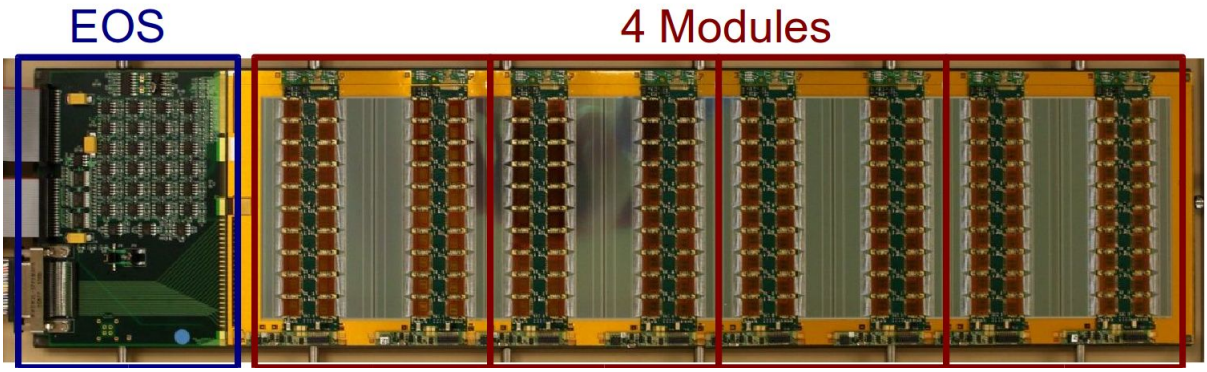


Figure 6: UK serially powered Stavelet

Figure 6 shows one of the single-sided Stavelets already assembled and used in the UK by several groups of the ATLAS strip detector upgrade collaboration. A double-sided Stavelet has been partially assembled at LBNL during this thesis, the so called US Stavelet, with the collaboration of others US groups. Although similar, there are key differences in the layout with the single-sided prototypes, described in section 3.6.

Apart from the Modules, the Stavelet hosts an End Of Stave (EOS) board. It is essentially a buffer board driving the Low Voltage Differential Signaling (LVDS) data lines. It permits the extraction of the data from each Module to the upper-level system, the High Speed Input Output (HSIO) and its interface board in our test case. The EOS board routes also the High Voltage (silicon sensor bias voltage) (HV) Power Supply (PS) lines. We will not enter in further details concerning this board and its communication protocols, as it is not a part of this thesis.

3.1 Silicon strip sensor

The silicon strip sensor is a silicon crystal. The sensor bulk is composed of p-type (doped) silicon. The back face has a p^+-type contact over the complete surface. The front face has n^+-type silicon strips implanted in the surface. An electric field is applied between the n strips and the backplane. Figure 7 illustrate such a sensor.

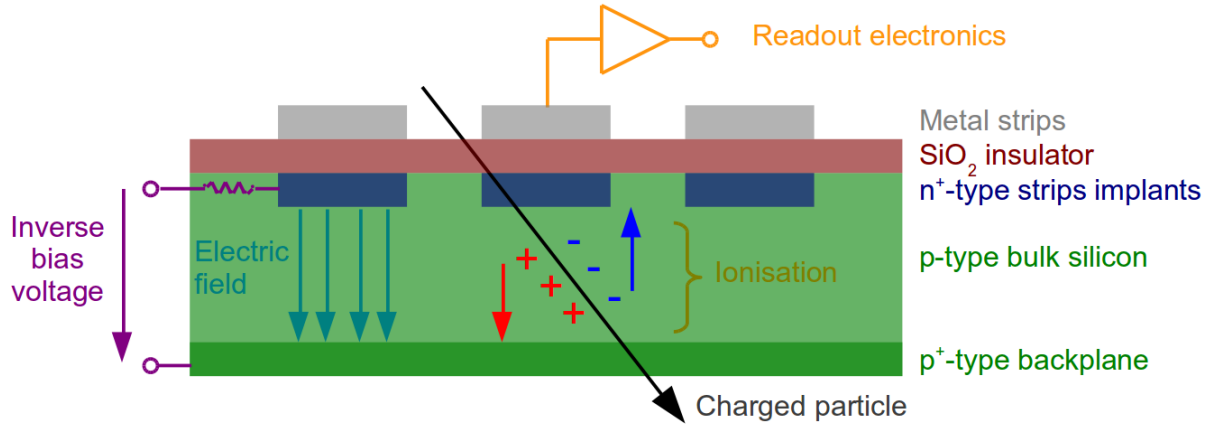


Figure 7: Section of a silicon strip sensor

When a charged particle passes through the silicon detector it creates ionisation in the bulk of the silicon. This frees electrons from the atoms of the silicon and leaves these atoms with an electron vacancy, an hole. The electrons drift in the electric field towards the positively charged n-type strips. The holes drift towards the negatively charged backplane.

The electrons are then collected by an n-type strip, which is connected to a sensitive electronic readout channel by AC-coupling. Metal strips, insulator and n-type strips form capacitors. By recording which channel fired, it is possible to determine where the charged particle passed through the detector.

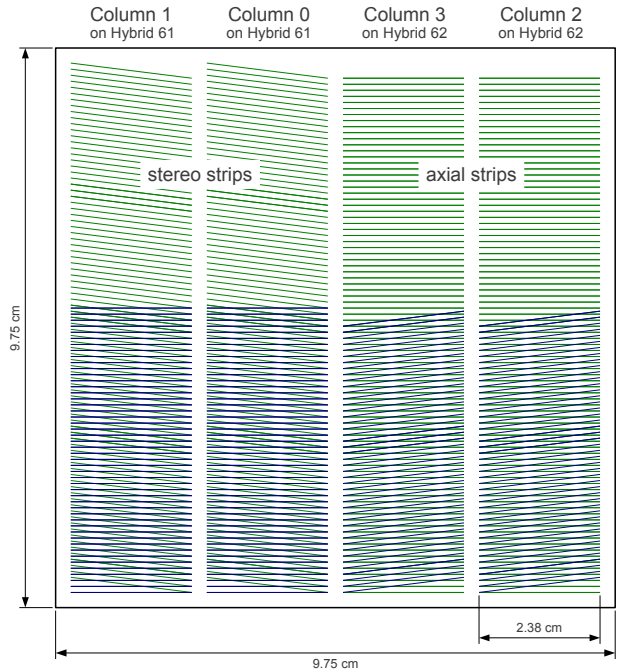


Figure 8: Silicon strips sensor layout

The sensor is a square of side $9.75cm$. It has a thickness of $320\mu m$. The strip pitch (distance between the center of two adjacent strips) is $75.6\mu m$. The 5120 strips, $2.38cm$ long, are organized in four rows, two of which are axially aligned, i.e. with the strips parallel to the edge of the sensor, and two of which

have stereo strips, inclined at an angle of $40mrad$. [LW10] This layout, represented on figure 8, allows a two-dimensional particle detection with two identical one-dimensional strip sensors. The green lines represent the strips. The blue lines represent the same strips, flipped, as it will be with two identical sensors, one on each side of a Stavelet.

3.2 Readout electronics

The readout electronic is composed by a pre-amplifier, a pulse shaper and an analog to digital converter. Figure 9 schematize it.

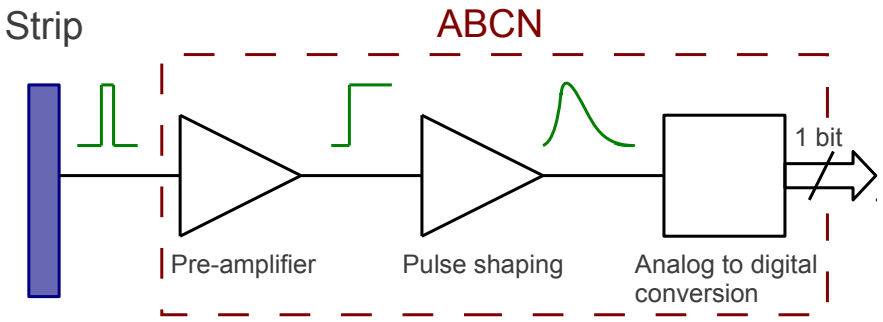


Figure 9: Schematic representation of a semiconductor detector readout electronics

The pre-amplifier is needed to measure the low charges (proportional to the particle energy, around $1fC$ in our case) at the detector output. Its design has to be optimised for low noise. The amplifier is configured as an integrator to convert the short current peak into a longer impulse. A pulse shaper is needed to improve the Signal-to-Noise Ratio (SNR). [Spi05] It defines the amplitude and length of the pulse generated by a particle. The detection rate depends on the pulse length. The digitizer converts the signal from analog to digital for further treatment. Depending on the requirements, the resolution can be one or more bits.

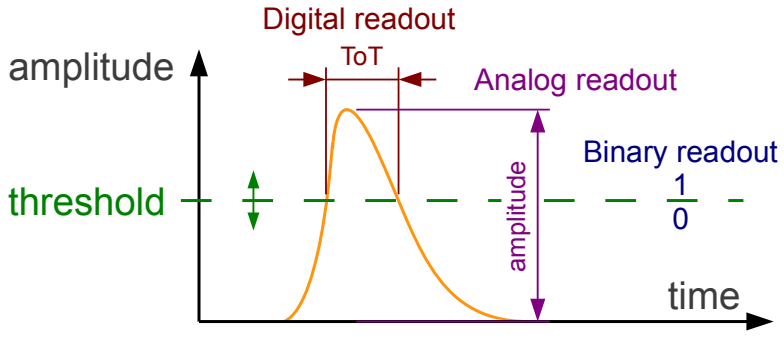


Figure 10: Readout techniques : analog, digital and binary

In order to simplify the readout electronics and to minimize the amount of transmitted data, the conversion is only done on one bit, indicating a hit or not. The digitalisation is done by a comparator with the help of a numerically controlled threshold voltage. This allow an optimal setting for every channel. This technique is named binary readout : if the pulse amplitude is higher than the threshold it is a hit, otherwise not. It exists two others readout techniques providing more information about the

particle charge : analog and digital readout. The analog readout measures the pulse amplitude and the digital readout measures the Time over Threshold (ToT). Figure 10 shows the measured parameters.

3.3 Module

The current Module prototypes consist of a silicon strip sensor with 5120 channels, forty readout Application Specific Integrated Circuits (ASICs) (ATLAS Binary Chip Nexts (ABCNs)) and two control ASICs for digital communication (Buffer Control Chips (BCCs)). Two flex Hybrid boards host the ABCNs. Each ABCN reads out 128 channels, and there is one BCC per Hybrid. The ABCN channels are connected to the sensor strips using wirebonds. The Hybrids are directly glued on top of the sensor. A Module built here can be seen on figure 11.

The Module and the two BCCs are mounted on a PCB Frame for individual testing purpose. It won't be present in the Stave. There are two types of Frame : one with DC-DC and the other with serial powering architecture. See section 3.4 on powering schemes. The serial Frame contains the AC-coupling capacitors. The DC-DC Frame hosts the two DC-DC converters. In the final design (if DC-DC powering architecture is chosen), they will be integrated on the Hybrids. By exchanging the two types of Frames on a Module, it is possible to make a comparison of Module performances between the two powering schemes.

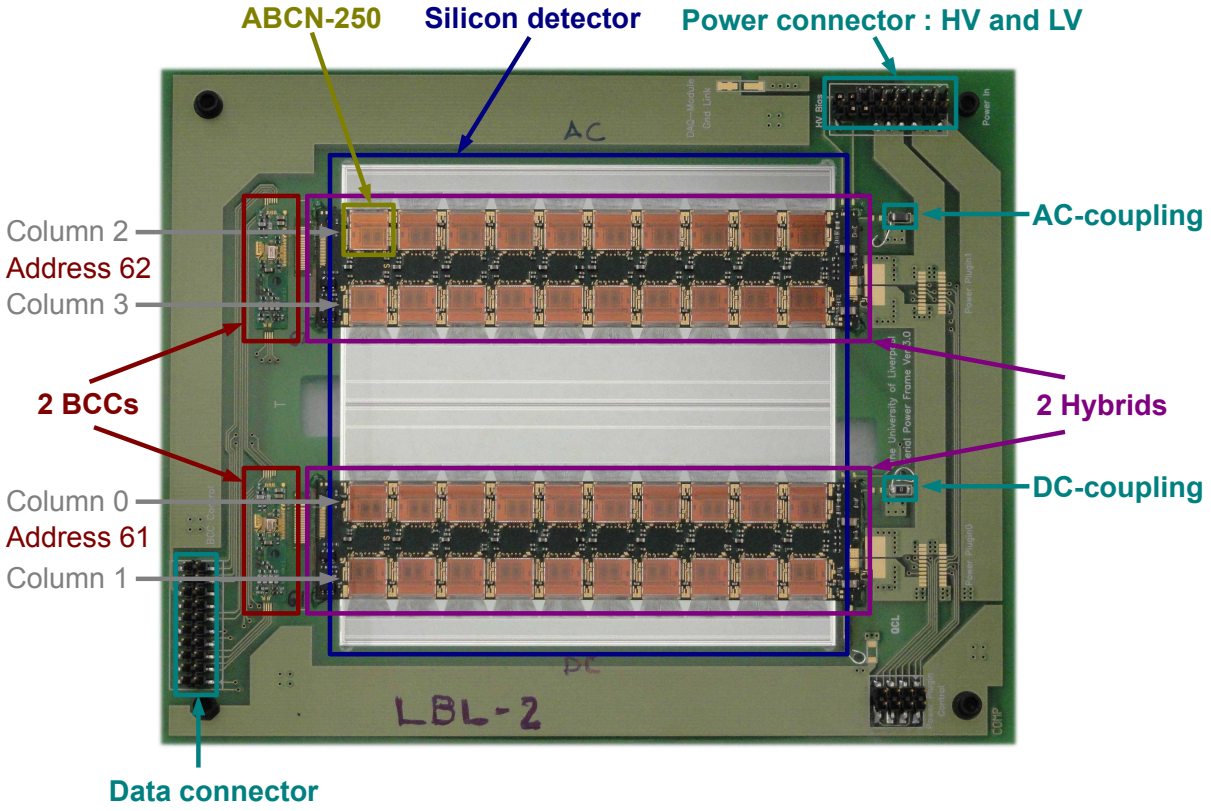
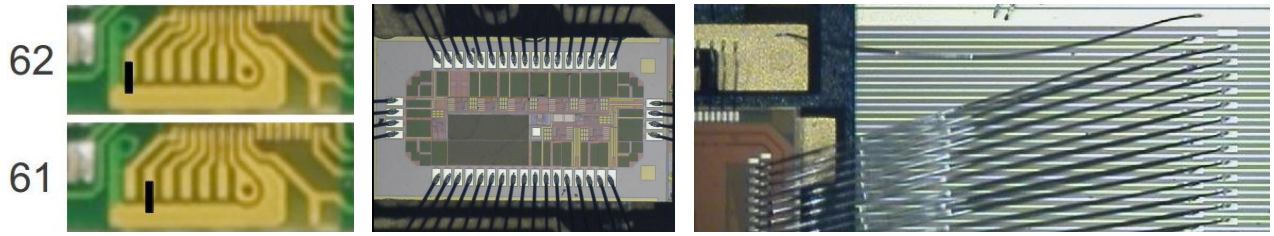


Figure 11: LBL-2 Module on a serial Frame

The Hybrid addresses, used by the test software and in chapter 5 to identify them, is hardware programmed by wirebonds on the BCC board. Addresses 61 and 62 are programmed as shown by figure 12(a). Hybrid 61 is connected to the strips columns 0 and 1, Hybrid 62 to columns 2 and 3. Wire-

bonding is extensively used to connect the ASICs to their board, the ABCNs to the silicon sensor and many others electrical connections. Some examples are shown on figure 12.



(a) BCC address (b) BCC : ASIC to board (c) ABCN : ASIC to board and silicon sensor

Figure 12: Wirebonding

The two ASICs are currently under design for a new version using a $130nm$ Complementary metal-oxide-semiconductor (CMOS) technology instead of $250nm$ actually. The upgraded BCC, so called the Hybrid Control Chip (HCC), will mainly increase the data transfer rate, reduce the power voltage and handle more triggers. The upgraded ABCNs will acquire 256 channels instead of 128 and will exhibit significantly lower power dissipation. Ten ABCNs will then be sufficient per Hybrid, reducing the material cost and permitting the integration of the HCC and eventually the DC-DC converter. We will not enter in further details concerning these ASICs and their data communication protocols, this is not a part of this thesis.

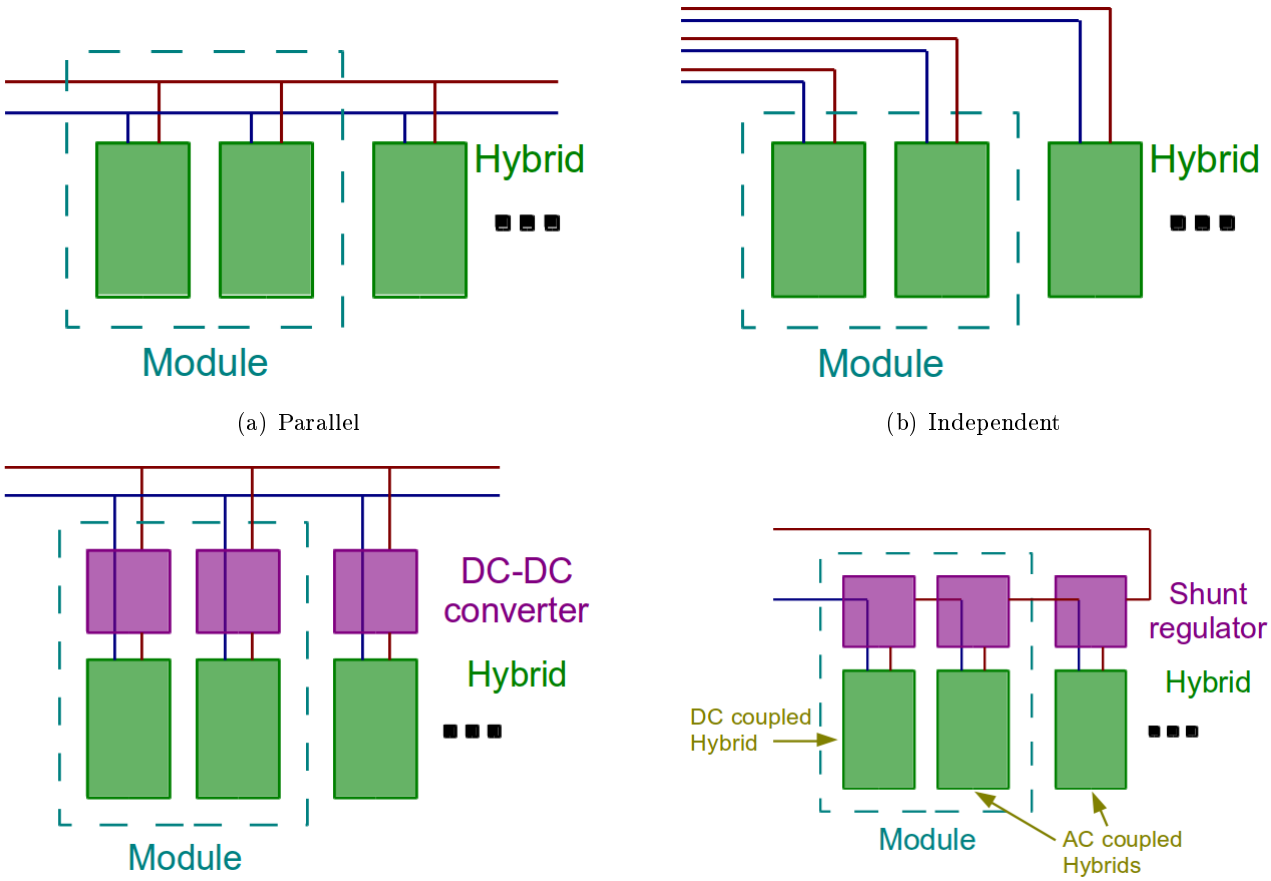
3.4 Powering schemes

We need to power all the Hybrids on the Stave with constant voltage. The first idea that come in mind is the parallel powering, represented on figure 13(a). Two lines with each Hybrid connected in parallel to them. Only two wires per Stave, good for the material cost. Each Hybrid has the same ground : this make easier the digital communication (no need of AC-coupling) and has actually lower noise. See the noise measurements in section 5.1. The drawback is that this two lines carry a lot of current, thus inducing power transmission loss by Joule heating through the power lines ($P = I^2 \cdot R$).

The solution adopted by the actual version of ATLAS is independent powering, represented on figure 13(b). It solves the transmission loss of parallel powering but increases the number of services, increasing the physical space used by them, the material cost and the number of power supplies.

Due to the increasing number of channels and Hybrids, independent powering is no more conceivable for the ATLAS upgrade. There is simply not enough place for all the wires. And we still want high efficiency, that means low current. The only way to go is to increase the distribution voltage. There are now two solutions. Parallel distribution with DC-DC converters converting the voltage down to the Hybrid level, represented on figure 13(c). Serial distribution with shunt regulators deviating the extra current to maintain a constant voltage on the Hybrid, represented on figure 13(d).

Due to the need of an inductor and a shielding box, the DC-DC converters increase significantly the material cost. On the other hand they allow all the Hybrids to be DC-coupled. With serial powering, only one Hybrid is DC-coupled, the others need to be AC-coupled, which can create additional noise. On the Module serial Frame, the Hybrid 61 is DC-coupled and the 62 AC-coupled, see figure 11. See the results on a single Module in section 5.1. There are ongoing work to reduce the converters material



(a) Parallel

(b) Independent

(c) DC-DC

(d) Serial

Figure 13: Powering schemes

and, on the other hand, to decrease the noise induced by AC-coupling.

There is another issue with the serial powering, called the double trigger noise. In the current design, the ABCNs store the hits they record on their channels in a buffer with an associated timestamp. Later, the high level software, outside of the detector, choose the interesting events and send triggers[2] to the ABCNs in order to get the interesting timestamps. The double trigger noise appear when you extract data from an Hybrid (all its ABCNs) out of the Stave in the same time its neighbour is measuring its channels.

In order to evaluate each of the proposed powering schemes in a larger scale, two single-sided Stavelet prototypes have already been constructed in UK, one configured for each scheme. The US Stavelet, partially constructed during this thesis, is double-sided. One powering scheme on each side.

3.5 Bus tape

The bus tape, shown on figure 14, transmits electrical power and signals between the Module and the EOS on the Stavelet Core.

[2]This is the level one trigger, three levels of triggers permit to reject more than 99 percent of the recorded data.

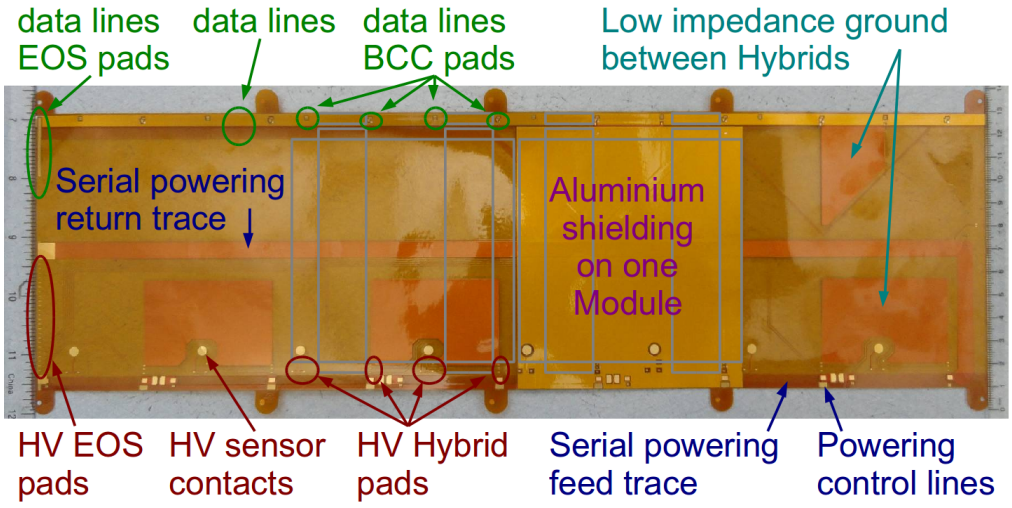


Figure 14: US bus tape

There is the BCCs data communication lines on top, bonded to the EOS and the BCCs. On the bottom are the PS distribution lines, the HV and the Low Voltage (supply the electronic on the Hybrid) (LV). This bus tape was developed for the serial powering scheme. For comparison purpose, we use the same bus tape for the Stavelet DC-DC side, cut the "serial powering feed trace" and "Powering control lines", and add an extra "DC-DC bus tape" (see section 3.12.

3.6 Core

The carbon-based Core is the thermo-mechanical assembly that holds and cools down the Modules. It also integrates the bus tape. The baseline Core design, used in previous Stavelet prototypes, is represented on figure 15.

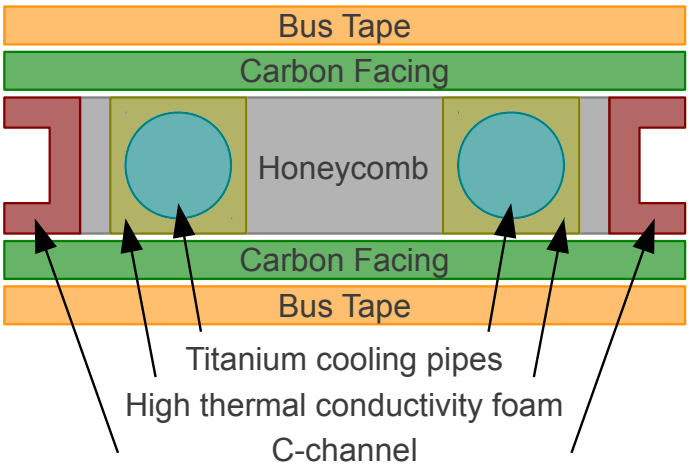


Figure 15: Baseline Stavelet Core design

The central part is a corrugated core of carbon fibre based Honeycomb with integrated titanium (steel on the actual prototype) cooling pipes surrounded by high thermal conductivity foam to achieve a

good thermal dissipation. The bus tape and the carbon Facing are co-cured together. This two are then laminated on the Honeycomb. The C-channel is the mechanical part permitting the end insertion of the Stave into the detector structure.

The carbon Facing is composed by three carbon fibre layers superimposed with perpendicular orientation (0°, 90°, 0°). The bus tape is composed by layers of different types : Kapton, Copper and Aluminium. To simplify the representation, we only represent three of them on figure 16.

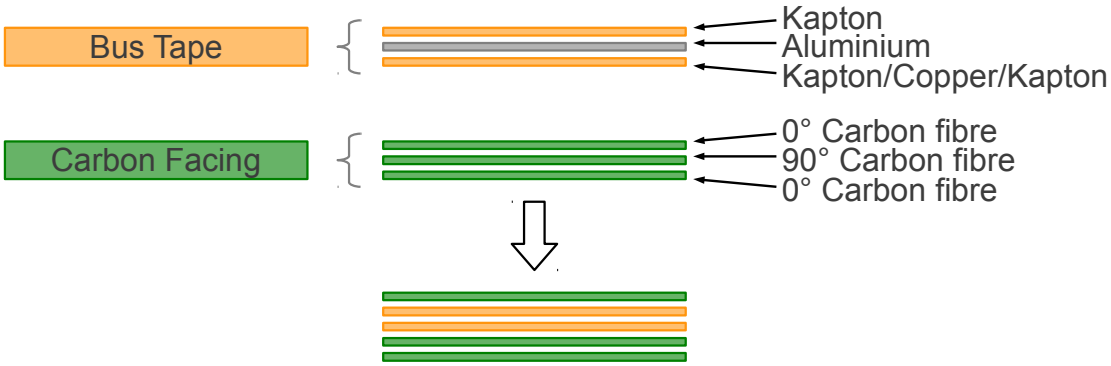


Figure 16: Tape and Facing decomposed

The idea for the US Stavelet is to combine the bus tape and the Carbon Facing layers by inserting the tape between two Carbon fibres, removing the aluminium layer to reduce the material present in the detector (about 10% of the Stave radiation length[3]). Reducing the amont of material on the passive components of the detector is critical : particles passing through passive materials are influenced by them and scatters from their original path, or are absorbed. Reducing the material inside the detector also reduces the influences on the particles and "fake" track. A side-effect is to reduce the weight of the detector and the material needed to support it.

The aluminium layer is a shielding between the sensor backplane and the bus tape data lines. For comparison purpose, we leave the aluminium on one of the Modules. We can see this special bus tape on figure 14. We will compare the noise between the aluminium shielded Modules and the others to see if this has a significant impact or not. This test was the motivation to build the US Stavelet, no other Stave without aluminium shielding exists. It is also the first double-sided Stave.

We can see on figure 17 the bus tape co-cured with the three carbon fibre layers. This work was done at LBNL composite facility.

[3]In physics, the radiation length is a characteristic of a material, related to the energy loss of high energy, electromagnetic-interacting particles with it.

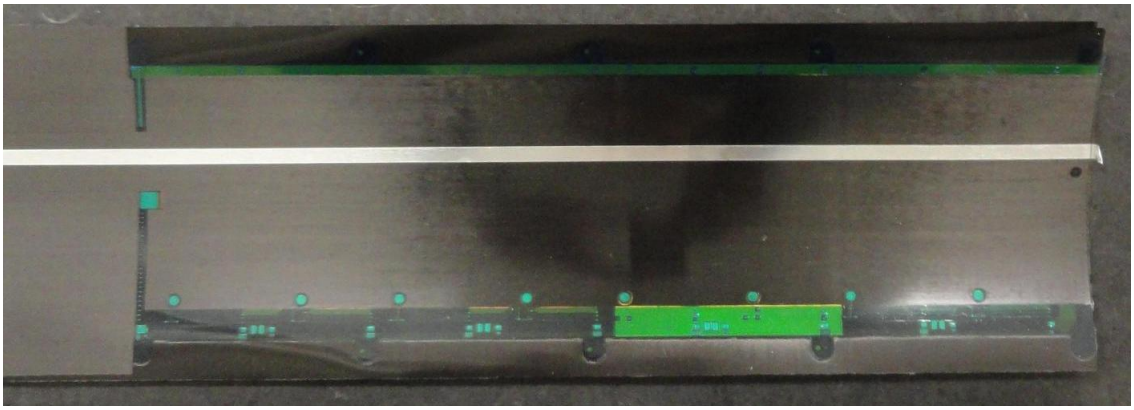


Figure 17: US bus tape co-cured with carbon fibre

Finally the insertion mechanism is different. The C-channels are replaced by Carbon Facing Side Pipes. This mechanical part is not further analysed in this thesis. The two carbon fibre shielding layers are then connected to ground. The actual representation of the US Core can be seen on figure 18.

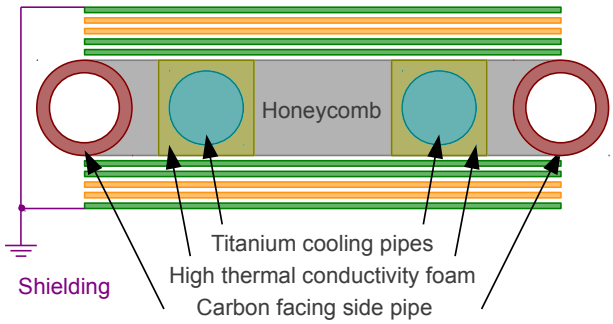


Figure 18: US Stavelet Core

Figure 19 is the actual Core of the US Stavelet prototype, assembled at LBNL composite facility. This prototype has stainless steel instead of titanium cooling pipes and metal / plastic inserts rather than carbon tube on its edges. These pieces host the DC-DC converters that will be integrated, if chosen, on the Hybrids. An aluminium line makes the connection to the outermost carbon layer, permitting to connect it to ground. Some mechanical precision measurements have been done after manufacturing. They are presented in section 3.7.

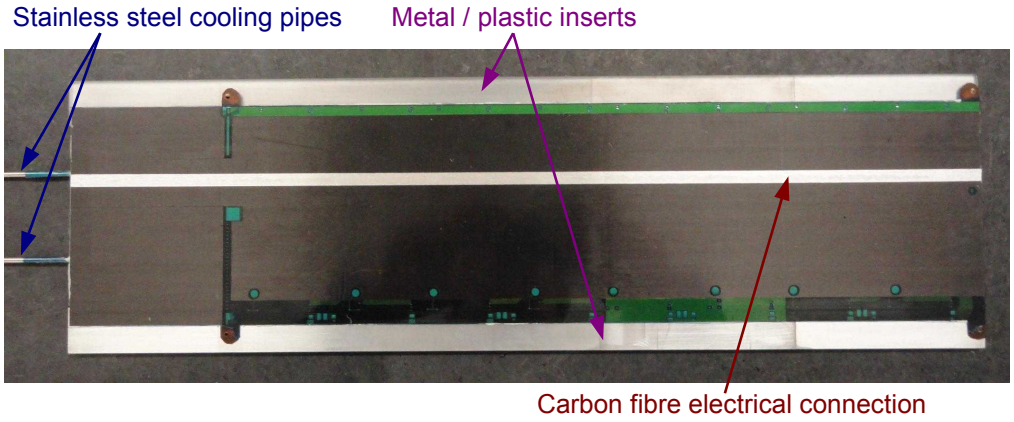


Figure 19: Stavelet Core after lamination

3.7 Mechanical measurements of the Stavelet Core

We have performed precision optical metrological measurements on the Stavelet Core to verify its dimensional accuracy after co-curing and lamination. Figure 20 shows the machine doing these measurements.

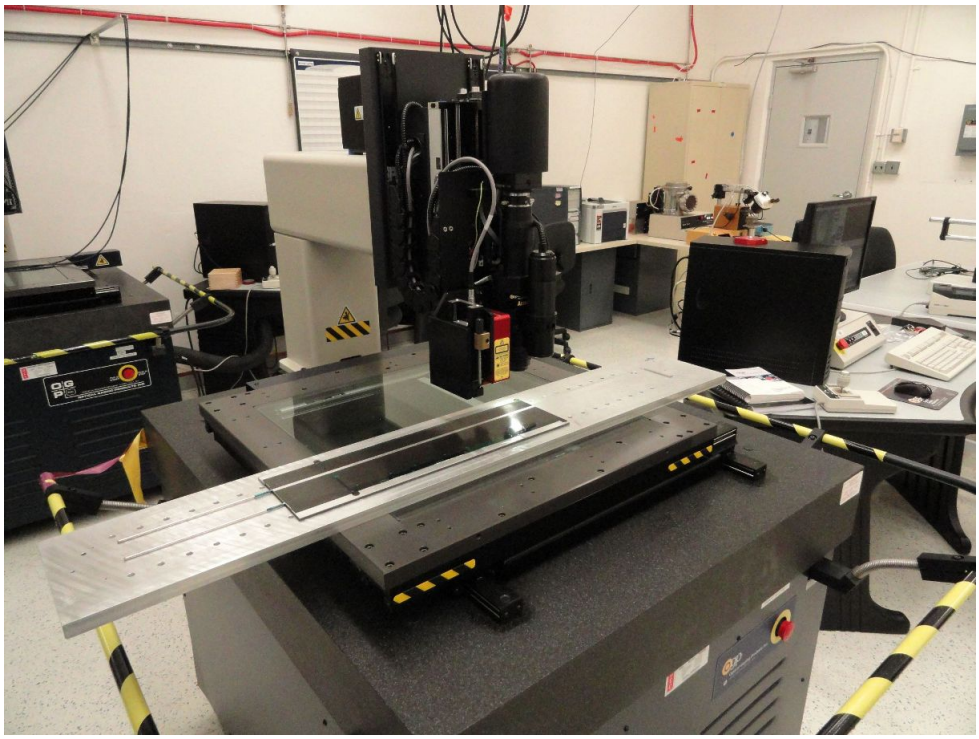


Figure 20: Optical metrological machine measuring the Core

We have measured many points on the Core. First the four reference holes that have been used during the assembly. We have then measured the bus tape HV contacts. These permit to see if the tape was deformed during manufacturing. Two plastic and aluminium pieces were added on each edge of the Stavelet Core, enlarging it to hold and give a higher thermal mass to the DC-DC converters. They are

used to fix the Stavelet inside its Frame too. It won't be present on the final Stave. To be sure the Modules will be correctly placed by the pick-up tool, we have to verify the parallelism of these pieces with respect to the tape. Figure 21 shows all the measurements done on the serial side of the Core and figure 22 is a plot of all these measurements. The raw measurements are shown in annexe C.

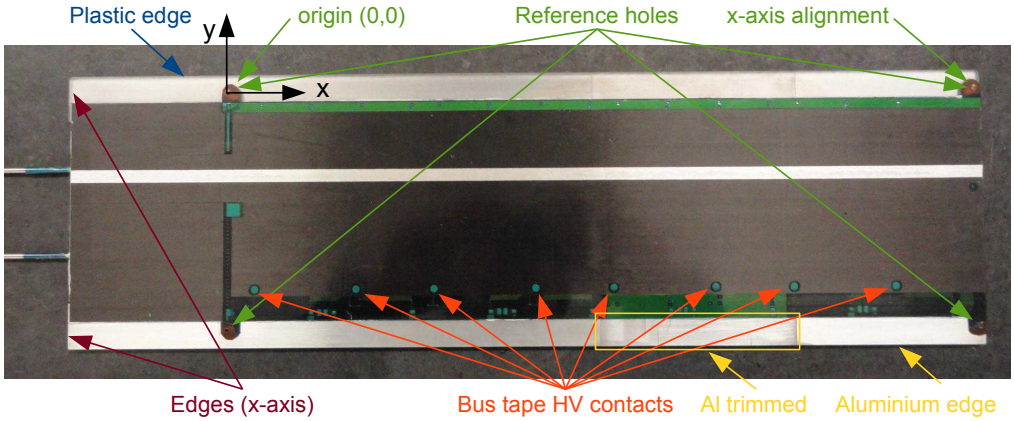


Figure 21: Measurement points on the Core

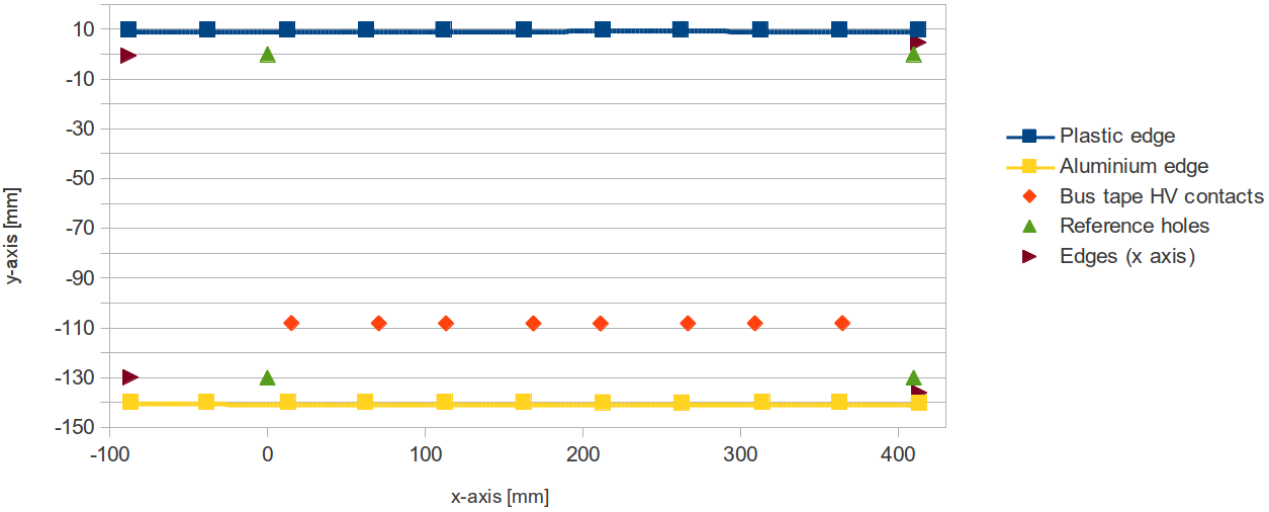


Figure 22: Core metrological measurements, serial side

Figure 23 presents in detail the position and diameter variations of the high voltage contacts on the bus tape.

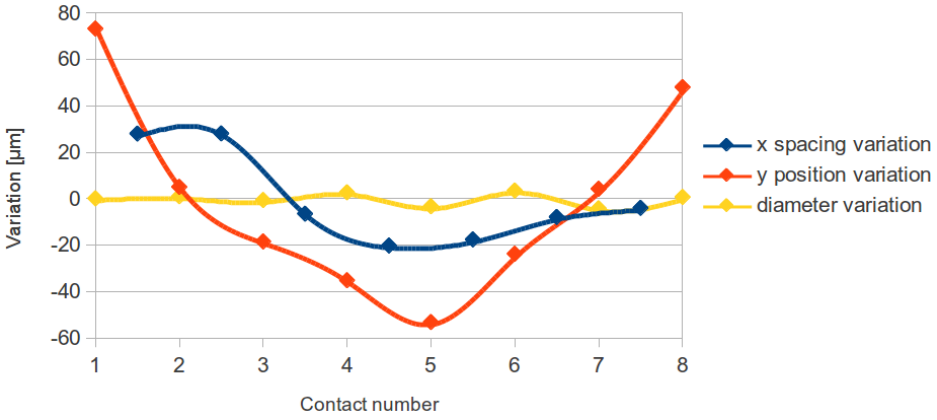


Figure 23: Bus tape HV contacts, serial side

The diameter variation is very small, only $7.7\mu m$ maximum. The spacings between the holes (x-axis) is nearly constant, $48\mu m$ maximum. The position on the y axis is less constant with a variation of $126\mu m$. The tape was deformed during the fabrication processes.

Figure 24 shows in detail the plastic edge (serial side point of view). Variations in the edge are within $170\mu m$

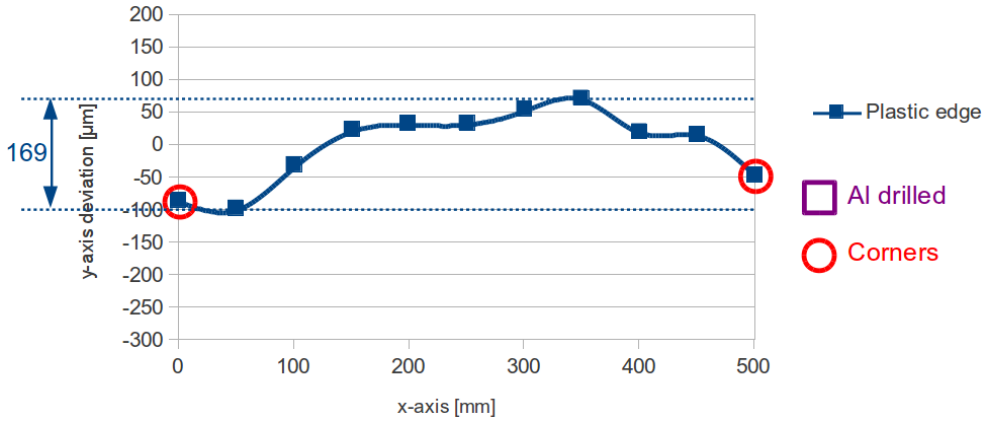


Figure 24: Plastic edge (from serial side) deviation

Figure 25 shows the aluminium edge. Here we can see three points out of range. One is a corner : it can be discriminated because the metal is never perfectly straight in the end. The two other points were measured on a trimmed region in the aluminium. As explained in section 3.6, the bus tape has aluminium inside it on one quarter. To compensate this extra height, the aluminium on the edge has been trimmed down. This default create errors in the measurements. Without this three errors, we are within $202\mu m$ deviation.

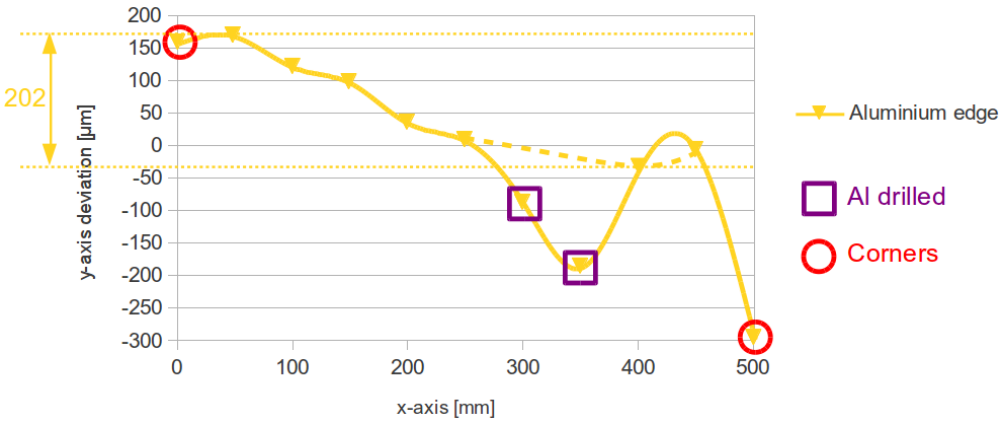


Figure 25: Aluminium edge (from serial side) deviation

3.8 Mechanical tools : Jig, Pick-up tool and Frame

We have designed three mechanical tools in order to pick the Modules and place them precisely on the Core : the jig, the pick-up tool and the Frame.

Figure 26 is a picture of the Jig, the Pickup-tool and a Module. The jig maintains the sensor in a known position, defined by three pins, by vacuum. The pickup-tool take the Module from the jig by vacuum on top of the ABCNs, leaving enough clearance for the wirebonds. The pick-up tool is placed on the jig with the help of four pins. The linear bearings allow it to slip down on the Core with the help of pins installed on the Frame.

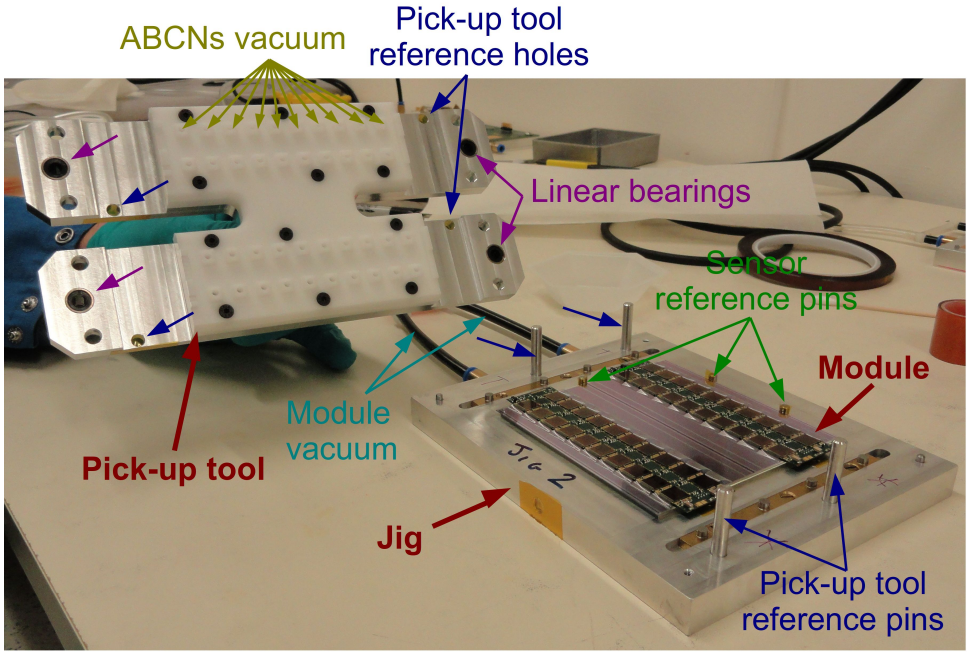


Figure 26: Jig, Pick-up tool and Module

Figure 27 is a picture of the Frame, the Core and two Modules on it. The Frame maintains the Core

in place with the help of nine pins on each side. The Core is laterally adjusted by set screws beside each pin. Sixteen pins, four per Module, are precisely placed on the Frame to locate the Modules. The linear bearings of the pick-up tool slip on them until the sensor backplane reaches the surface of the Core.

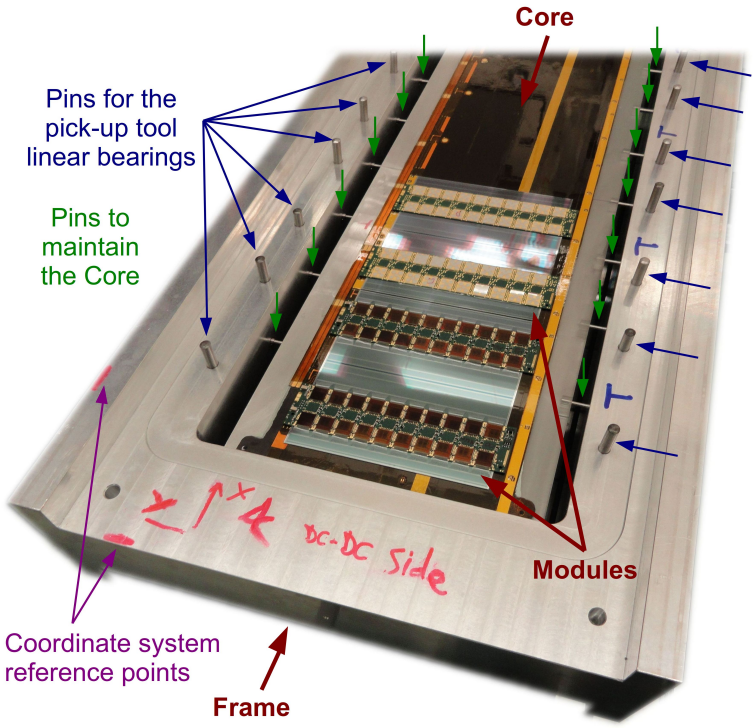


Figure 27: Frame, Core and Modules

3.9 Module positioning

On the Stavelet Computer-Aided Design (CAD) drawings, the Modules are positioned with respect to a reference pad, shown on figure 28 as seen by the optical metrological equipment (figure 20).

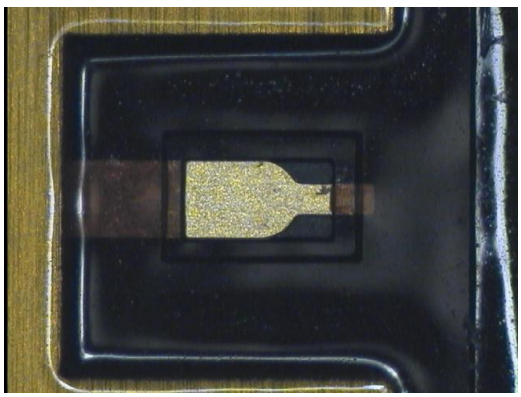


Figure 28: Core reference pad for Module positioning

The Modules is placed on the Core by the pick-up tool, using linear bearings for its positioning. The pins that will go through the bearings have to be placed on the right place in the Frame in order for

the Modules to be correctly positioned according to the reference pads. Holes will be drilled by tacking references on the Frame. We have to quote them from the Frame.

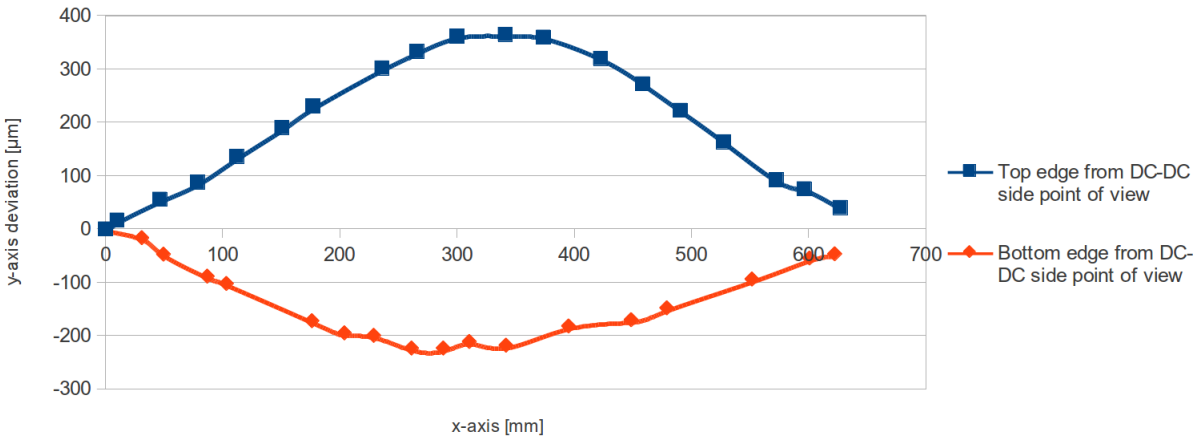


Figure 29: Top and bottom Frame edges, DC-DC side point of view

Figure 29 shows that the Frame edges have an offset up to $350\mu m$, so we cannot align the Frame edge in a milling machine and just move the machine x-axis. We will never be sure where this axis is really. To construct an axis system, we need three points : x zero, y zero and axis alignment. With a Computer Numerical Control (CNC) milling machine, it is easy to enter these three points as a basis and to drill the holes according to this coordinate system and not the machine one.

With an optical measurement equipment these three points can be taken to construct a basis. We just need to take the same ones as the machine shop. Two of them are visible on figure 27 in red. So we take this three points and make them our basis. Then we measure the position of the four reference pads (one per Module) with respect to this basis. We can get the linear bearings pins location relative to the reference pads from the Stavelet and the pick-up tool CAD drawings. Then get the bearings pins location with respect to the Frame basis and send them to the mechanical shop for machining. All these points are printed on figure 30 for the DC-DC side. The serial side is similar.

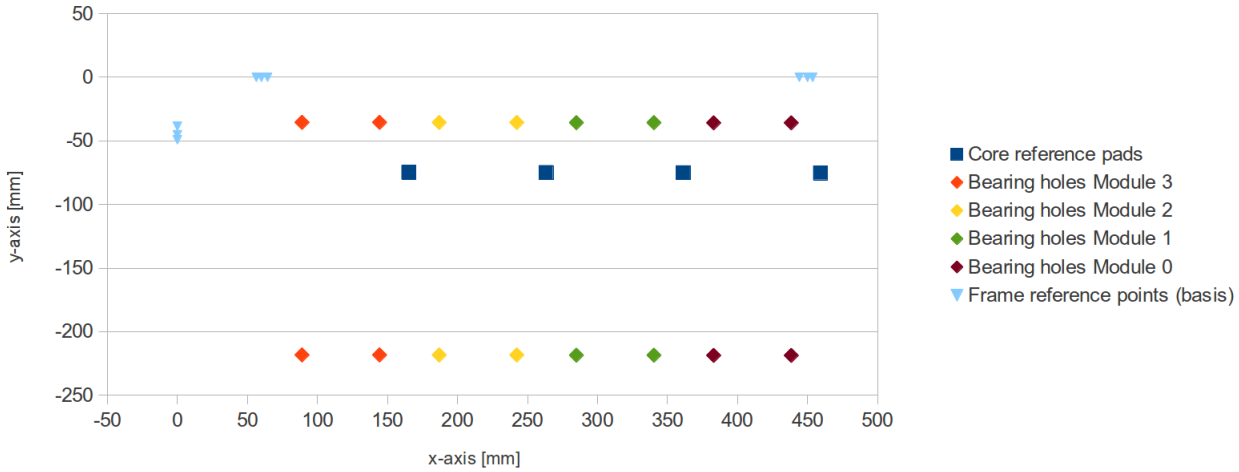


Figure 30: Linear bearings pins location, DC-DC side

We can take the opportunity to survey the reference pads position. The deviation in all axes (x,

y and z) are printed on figure 31. The distance variation between pads is less than $50\mu m$, which is acceptable. We observe also that the reference pads are not aligned with the chosen x-axis on the Frame. That doesn't matter, it's precisely why we calculate the pins position according to the reference pads position. We observe variation in height too. If we remove the second pad, which is below the aluminium shielding[4], it matches well a linear interpolation. That means the Core is not horizontally positioned into the Frame. The linear bearings allowing a vertical movement, it is not a problem. The same analyse has been done with the serial side with similar results.

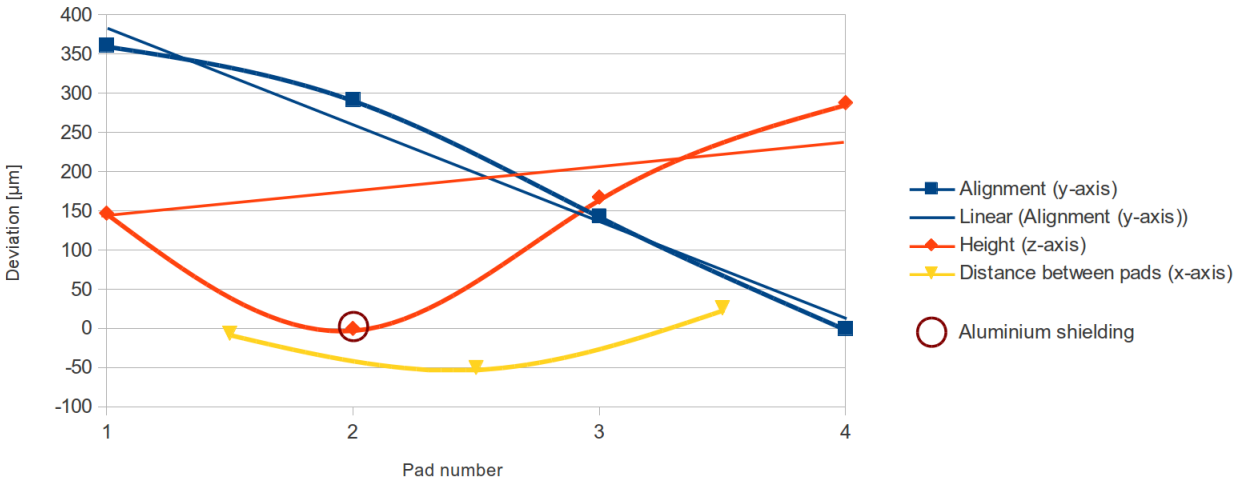


Figure 31: Reference pads position analyse, DC-DC side

The reference pads position helps us whenever we need to reposition the Core inside the Frame. For example after the bonding, soldering, cleaning etc. An example of the Core displacement after a repositioning is shown on figure 32.

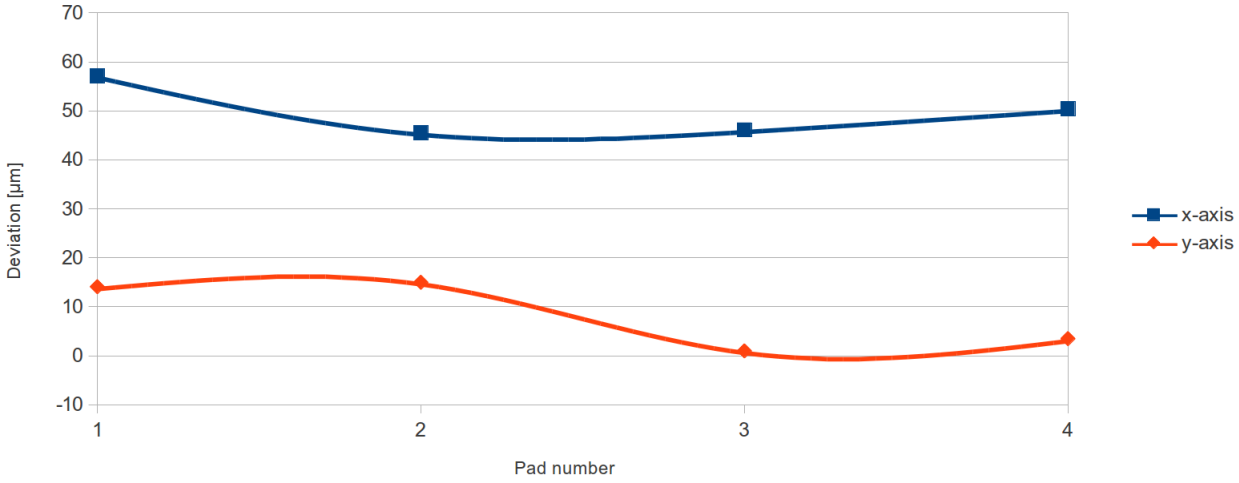


Figure 32: Absolute Core displacement after a repositioning

[4]See figure 14 of the bus tape. The aluminium layer add extra height on a portion of the tape. The honeycomb and the inserts have been milled for the top to be flat. That explains why this pad is below the others.

3.10 Module gluing

On figure 33 we can see the glue pattern on the Core, just before we put a Module on it.

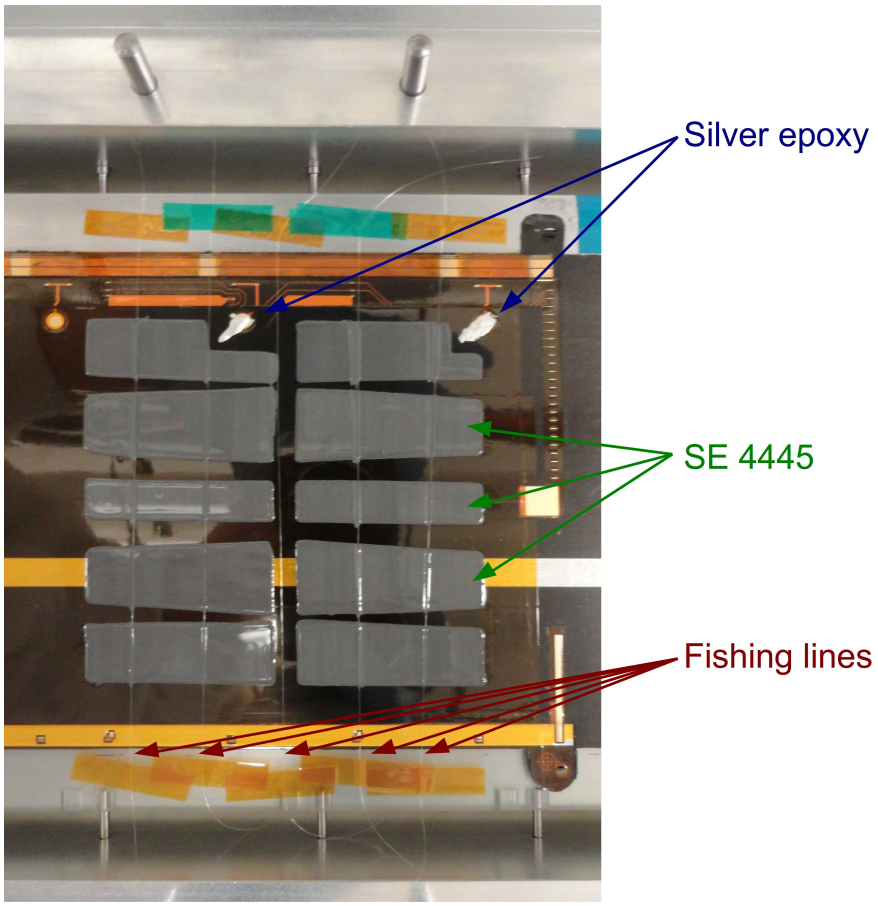


Figure 33: Glue pattern : SE4445, silver epoxy and fishing lines

The main glue is the SE4445, an electrical insulator and a thermal conductor. We need an electrical insulation to isolate the sensor backplane (bias voltage of up to $-500V$) from the Core facing carbon fibre, which will be the shielding, connected to the ground. A good thermal conductivity is needed to evacuate the heat from the Hybrids to the Core integrated cooling pipes. The glue as to be resistant to radiation, which can be critical. Studies were conducted to determine the most appropriate glue with respect to this criteria, among others. (for example [CVG02]) The pattern was applied by a "blue tape" mask, designed in UK.

Another glue is the silver epoxy, electrically conductive. Its goal is to make a contact from the bus tape HV pads to the sensor backplane. There is two pads for redundancy. To isolate the pad from the carbon fibre, we applied a kapton insulation layer on all the Core, taped down to the gold pad. See figure 34.

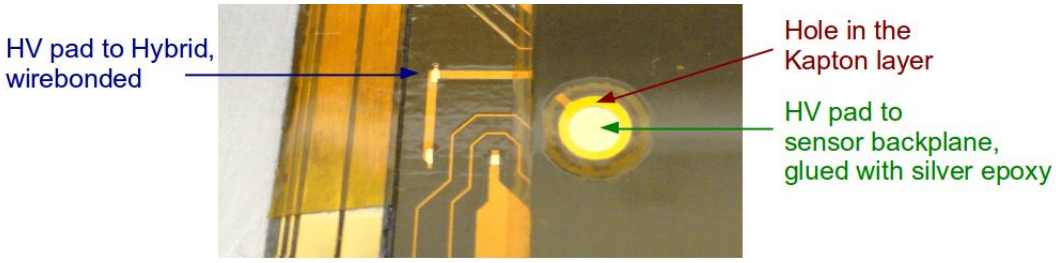


Figure 34: HV pad on bus tape, before applying silver epoxy

Finally we add five $125\mu m$ diameter fishing lines to control the distance between the sensor backplane and the Core. As these insulation layers (SE4445 and kapton) between conductive layers (sensor silicon backplane and carbon fibre) act as a capacitor, it has to be well controlled for reproducibility. These fishing lines may also allow the sensor removing by cutting the glue.

Before gluing a real Module on the Core, we have down two glue trials to determine the right amount of glue to put in the mask. The amount of glue is controlled by its height (his surface is fixed), itself controlled by the number of "blue tape" layers ($80\mu m$ each). We spread the glue inside the mask holes with the help of a razor, so its thickness is the same as the mask. Figure 35 shows clearly than a three layers "blue tape" mask is the best option.

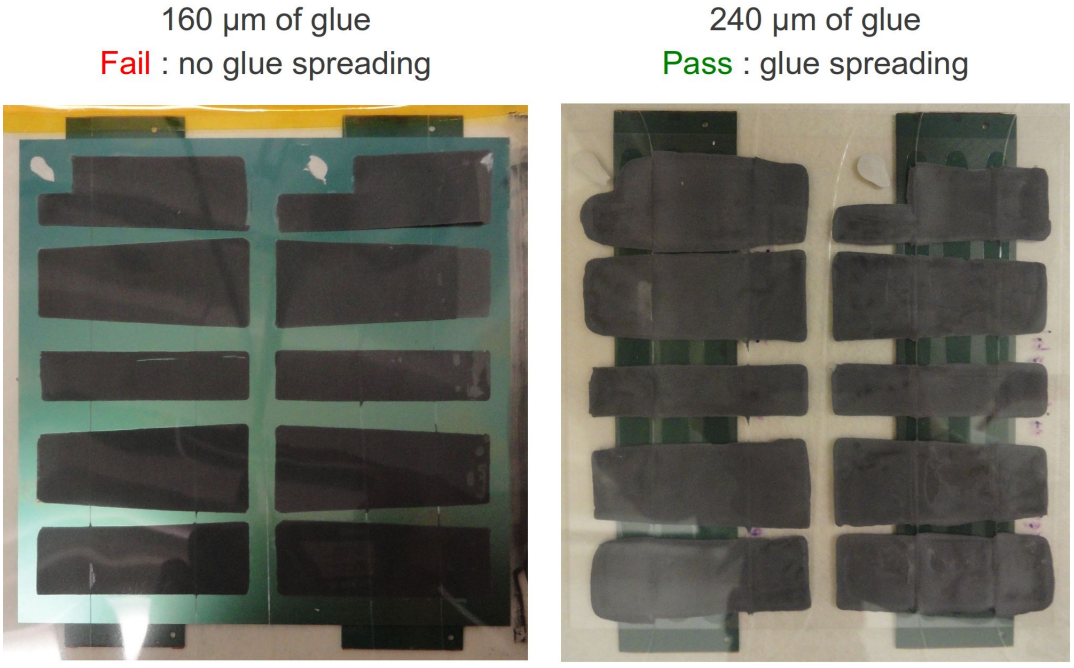


Figure 35: Two glue trials : one successful, the other unsuccessful

After determining the glue amount and applying it with the pattern shown on figure 33, we put a Module on it with the help of the pick-up tool. See figure 36. The linear bearings allow no horizontal movement, fixing the Module position. They allow a vertical movement, permitting us to slip the Module down to the fishing lines. Then we put some height on it and wait eight hours for each glue to co-cured.

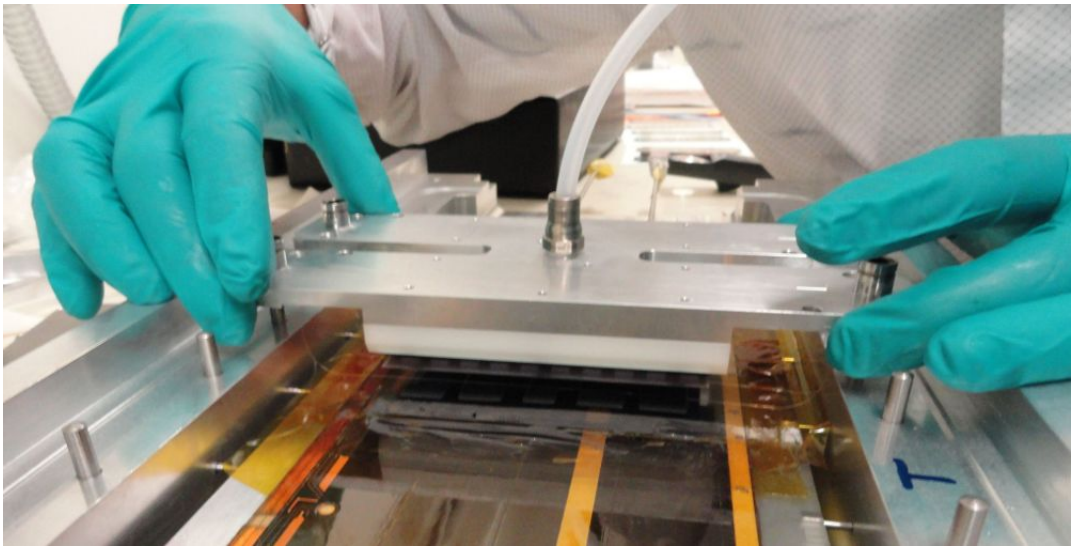


Figure 36: Placement of a Module on the Stavelet Core

3.11 Gluing results

Figure 37 shows the first Module (LBL-5) glued on the Stavelet after the removing of the pick-up tool.

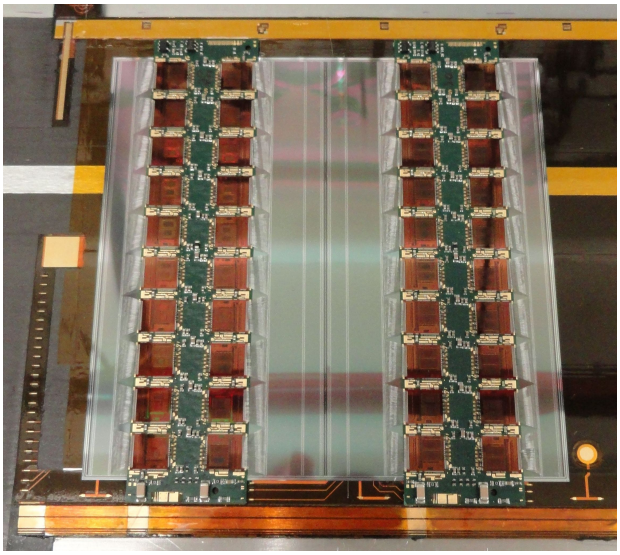


Figure 37: First Module (LBL-5) glued on the Stavelet Core

The Module is well positioned. Figure 38 shows a zoom on the HV and ground bonding pads of each Hybrid, all well aligned with the pads on the bus tape. The results are very similar for the second Module (LBL-3).

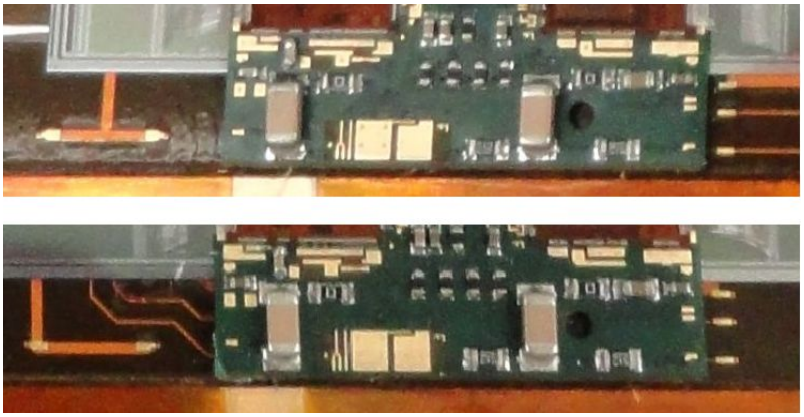


Figure 38: All bonding pads well aligned

Of the two HV pads, only one makes contact to the sensor backplane on LBL-5. The two make contact on LBL-3.

During the electrical testing of LBL-5, we have seen a bias current much higher than expected. After visual inspection, we found a scratch on the sensor bias ring, illustrated by figure 39, opening the guard rings that separate the active region of the detector to the edges of the crystal, thus allowing a leakage current path. It seems to have been caused by a metallic tweezers. We don't know exactly from where it comes, but it was already present right after the pick-up tool removing. We can easily see it on figure 38, bottom picture. We have no possibility to fix it, the Module sensor is definitely broken. At least it won't compromise the test validity. We can still run the Stavelet with only three working Modules or maybe remove it. There were no damage on the second sensor, the LBL-3.

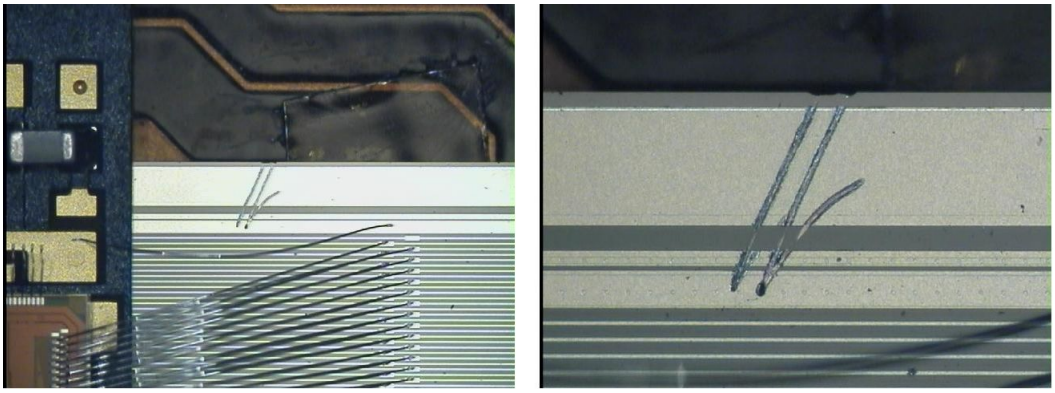


Figure 39: Scratch on LBL-5 bias ring

3.12 Additional work

We have also glued the BCCs, for digital communication between the Hybrids and the EOS, and the DC-DC converters (this side of the Stavelet use the DC-DC powering scheme). The EOS was also fixed by double-sticky tape.

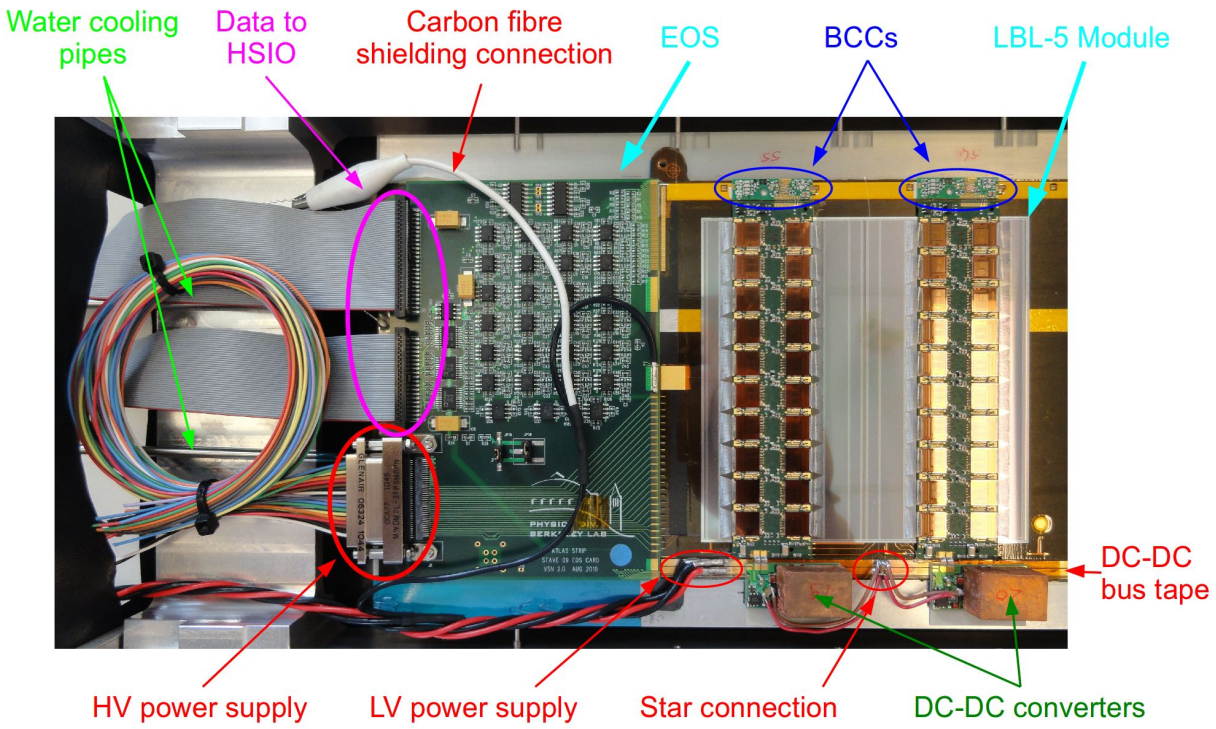


Figure 40: Additional components on the Core

An additional "DC-DC bus tape" was also glued in place of the original "serial powering feed trace" and "Powering control lines" (see figure 14). It has two thick copper traces for power distribution and two thin for the 1-Wire bus[5]. This bus is used to power ON and OFF each DC-DC converter individually, allowing us to start or stop an Hybrid from SCTDAQ.

The thick LV wires were soldered directly on the "DC-DC bus tape", bypassing the EOS to avoid Joule heating. The DC-DC converters were also connected to the bus tape by wires instead of wirebonds, using the "Star connection". An alligator clip was also added to permit the connection or disconnection of the carbon fibre shielding layer to the ground. It will be useful for comparison purpose.

All the wirebonds were done by our technician, Rhonda Witharm. The majority of them transport data : BCC to Hybrid, BCC to bus tape, DC-DC converters to bus tape, EOS to bus tape. Some others carry power (HV and LV) : Module to bus tape, DC-DC converters to Module.

Finally the cooling pipes are connected to the water chiller. The LV is connected to a commercial PS, the HV to the SemiConductor Tracker High Voltage (SCT HV) power cards, controlled by a custom software presented in section 4.2. The data Input/Output (IO) are connected to the HSIO, operated by a computer software for data injection and analysis. There is 4 Modules ·4 rows ·10 ABCNs ·128 channels = 20′480 channels to measure on each side. The test systems are described in chapter 4.

[5]1-Wire is a device communications bus system designed by Dallas Semiconductor Corp. that provides low-speed data, signaling, and power over a single signal.

Figure 41 shows the actual state of the Stavelet with two glued Modules.

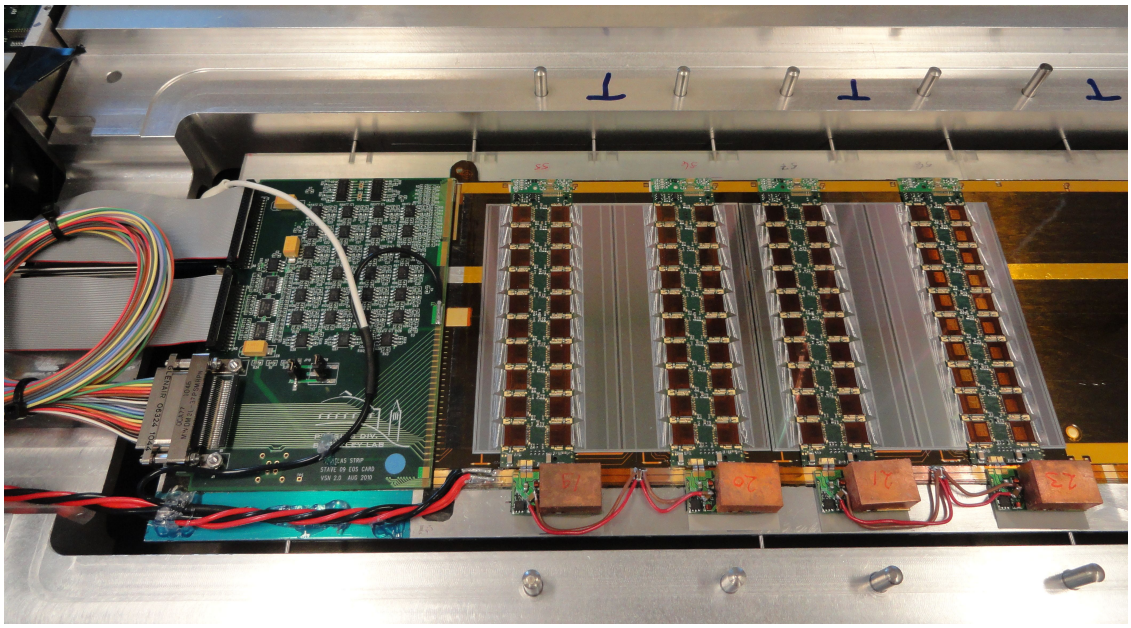


Figure 41: Stavelet with two glued Modules

4 Test systems

The test systems are the hardware and software we use to test the Modules and the Stavelet. Some of them have been built, developed or tested during this project. We will first go through the test setups, then the developed LabVIEW control software and finally the noise measurement method.

4.1 Module and Stavelet test setups

Figure 42 shows the Module test setup, installed and used last year by Niklaus Lehmann during his bachelor thesis. [Leh11] Figure 43 shows the inside of the Module test box and figure 44 the Stavelet test setup with its test box.

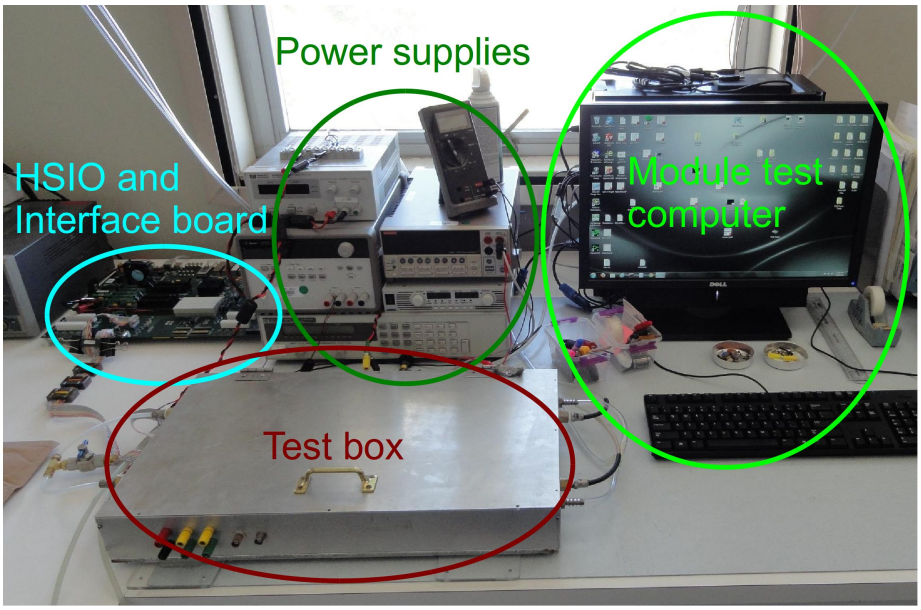


Figure 42: Module test setup

Water cooling : cold water (3 to 6 °C) flows through the Stavelet Core cooling pipes or through an aluminium cooling block which makes contact with the silicon sensor backplane. The goal is to cool the ABCNs down through the Hybrids and silicon sensor and to control the sensor leakage current. The temperature must be as constant as possible, the sensor performances being very sensitive to this parameter.

Nitrogen : the gas is injected in continuous to drop humidity and prevent moisture.

Test box : The test box protects the Module or the Stavelet from physical damage and light, and allows a dry nitrogen atmosphere. There is opening for the water cooling, the nitrogen, the power and data lines.

HSIO : The High Speed IO board is a generic DAQ board with a large number of modern input/output signal types and central processing control with a Vertex-4 Field Programmable Gate Array (FPGA). It was initially designed for and has been in use extensively at the Linac Coherent Light Source facility. Its generic capability has found applications in various silicon tracking upgrade projects in ATLAS. The board is connected to the test PC by Ethernet and to its

interface board by a custom connector.

Interface board : this board connects the HSIO either to the EOS (Stavelet test setup) or to a buffer board (Module test setup), itself connected to the Module Frame.

Test computer : holds the measurement and control software, and program the FPGA present on the HSIO board.

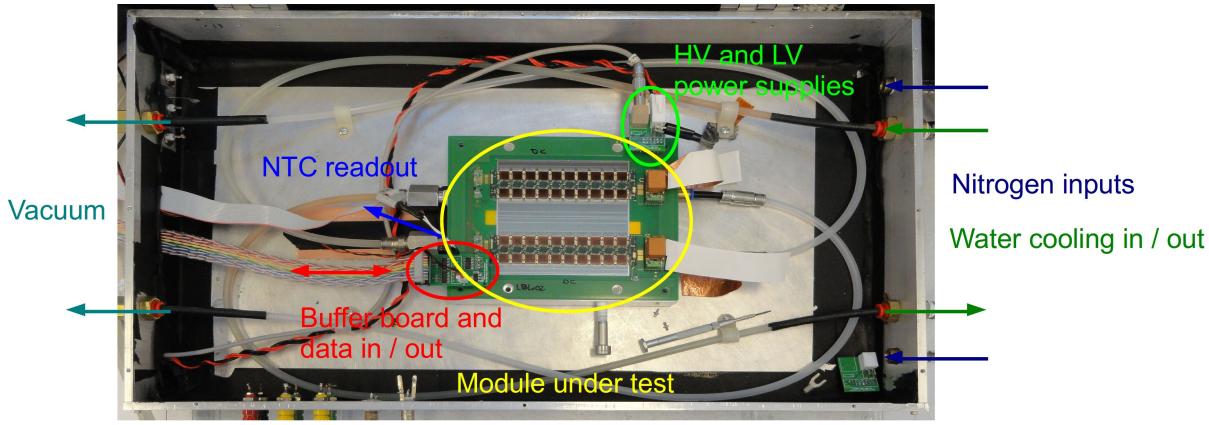


Figure 43: Module test box

The following items are only present on the Module test setup :

Vacuum : is used to maintain the silicon sensor down to the aluminium cooling block.

NTC readout : measure the temperature of an Hybrid to prevent overheating.

Buffer board : ensure the communication between the BCCs and the EOS interface (connected to the HSIO board). On the Stavelet this link is assured by the EOS.

Module Frame : Support the Module under test and the BCCs. There is one type of Frame per powering scheme : the serial Frame and the DC-DC Frame.

Module under test : the Module currently tested. It can be a DC-DC or a serially powered Module, depends of the Frame where it is installed. If DC-DC, like on figure 43, the DC-DC converters are mounted on the Module Frame.

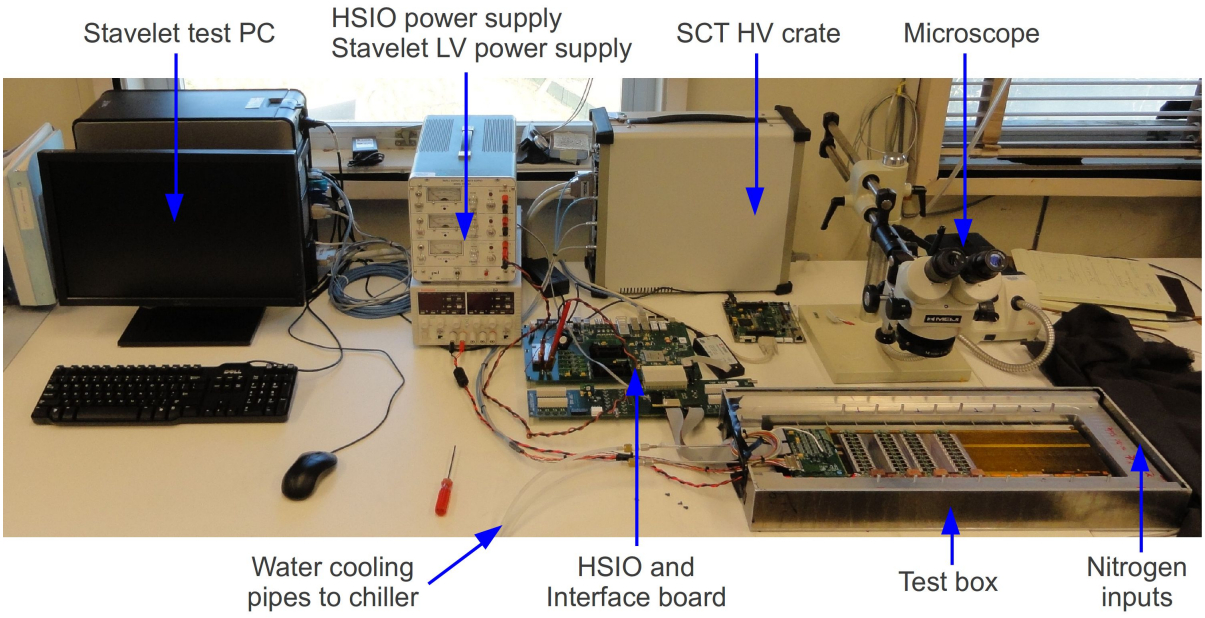


Figure 44: Stavelet test setup

HV PS : silicon sensor bias voltage, $200V$, less than $10\mu A$. Provided by a Keithley SourceMeter for the Module test setup and two SCT HV four channels cards for the Stavelet test setup. They are controlled by the Stavelet HV controller LabVIEW software (see section 4.2) developed for this use case.

LV PS : power the Hybrids, $10.5V$ and around $2.5A$ per Hybrid for DC-DC powering, $5A$ and around $6V$ per Hybrid for serial powering. Two PS for the Module test setup (one for serial powering requirements, the other for DC-DC powering requirements). One two channels for the Stavelet test setup, able to power the DC-DC and the serially powered side simultaneously.

HSIO PS : Power the HSIO. One PS per setup.

Buffer board PS : Only for the Module test setup.

4.2 SCT HV controllers

The SCT HV controllers are three programs created during this project to aid the test of the Stavelet.

To test the Stavelet, we need to power the eight Modules it contains. We need a high voltage ($200V$) to deplete the silicon sensor junction, the bias voltage. We don't have eight power supplies capable of this, and buying them is too expensive. The solution is to reuse two old SCT HV cards from the original version of the ATLAS detector. We first need to bring them back into service (cards are from 2001 and were abandoned in the lab), then understand the communication protocol to finally create our own control software that meet our needs.

The VME SCT HV PS is designed to provide the bias voltage for ATLAS SCT Modules. The HV203 model is a 1-unit wide, 6U height standard board. It houses four fully isolated channels and VMEbus interface. The system provides digitally controlled stable bias voltage in $0 - 500V$ range and a precise measurement of the output current. The maximum load of each channel is $5mA$. A current trip limit

can be set independently for every channel in the range from hundreds of nA to the maximum of $5mA$. Another parameter which can be selected individually for each channel is the ramping speed with which the nominal voltage is changed. [SCT04]

This card is mounted in a VMEbus crate. So we first have to communicate from the PC to this bus. We have here National Instruments PCI-MXI-2 and VME-MXI-2 cards. We can use them through the National Instrument Virtual Instrument Software Architecture (NI-VISA) programming interface to have access to the VMEbus from LabVIEW. The cards and drivers installation are explained in section B.1.

4.2.1 Requirements

The software must be capable to control independently and simultaneously the powering of the eight silicon sensors present on the Stavelet. The final voltage and a current limit can be set individually for each channel. IV curves can be printed. The program must be user-friendly and easy to use.

4.2.2 Communication protocol

The communication protocol has been retrieved by retro engineering of the existing designer C example code. The original code can be found in [SCT04].

The VMEbus is a register based communication protocol. That means you write a value to a specific register address, for example writing 0xD at 0x2A.

The first byte to write is the data length, in bytes, at address 0x0D. The second byte is composed of the channel number and the command number. The two less significant bits represent the channel number : 0 to 3. The bits 4 and 5 represent the command. The destination address depends on the command. The table 1 summarize this. The following bytes are data, only present in the case of a set command.

Command	**Binary representation**	**Destination address**	**Remark**
stop	00	0xD	Stop the selected channel
start	01	0xD	Start the selected channel
set	10	$2 \cdot CHN + 1$	Set the configuration (voltage, current limit and ramping rate)
read	11	$2 \cdot CHN + 1$	Read the status (voltage, current, flags)

CHN represents the channel number : 0 to 3

Table 1: Card commands

The transformation from user readable data (decimal voltage, current etc.) to the internal data representation of the card and vice-versa is complex. For example we have to calculate the current limit for the four probe resistances. It makes no sense to describe this here with words, it will be clearer to understand with the corresponding LabVIEW subVIs : *User2bytes.vi* and *Bytes2user.vi*.

4.2.3 Program architecture

The top-VIs have been developed with a producer-consumer pattern (except for the *Single channel controller*, it does not need it). There is multiple threads for event capture, display and processing. This offers an always responding application from the user point of view. The user events (button press for example) are captured and if an action is mandatory, it is queued in a buffer. A state machine dequeue the actions and process them sequentially. The read values are queued by the processing thread and dequeued by another thread for display. Inter-threads communication has been implemented. This has be done with the help of queues and notifiers. Semaphores were used to prevent concurrent access to the hardware.

The controllers were integrated in a single LabVIEW project and built as separate applications. They share the same subVIs. An application is a Windows executable instead of a LabVIEW Virtual Instrument (VI). It is possible to launch them without the LabVIEW development environment and to use them as regular applications, without the LabVIEW specific menus and buttons that the user don't care about. This give cleaner and more user-friendly controllers.

Multiple windows application was develop to enhance the user experience. Remote control has been implemented to open and close a window from another one. A window is a front panel in LabVIEW terminology. Each front panel require a VI. So the application is spread over multiple VIs. When they are all in the same application, they are no more than separate threads. The same communication processes can be used.

The controllers functions are split in many subVIs to increase the source code readability and reusability.

Write_to_card : Send a command and eventually data to the selected channel.
Read_channel_status : Read the status of the selected channel : voltage, current and flags (over-current, over-voltage, unrecognised command, unstable voltage). Use the *Write_to_card* function to send the read command.
User2bytes : Transform the user inputs (voltage, current limit, ramping rate) to the card internal representation. The results will be send via the *Write_to_card* function.
Bytes2user : Transform the bytes read by *Read_channel_status* to user readable data : voltage, current and flags.
Channel_control : Allow the entire control of a channel : start, stop, set configuration and read status. It uses the four pre-mentioned subVIs and are used for all further card access.
Read_average : Perform three reads and average the values.
Ramp_measure : Perform the ramping, compute the next step, stop for measurement (using *Read_average*), stop ramping when final voltage reached. Quit at any time if a stop is requested by the top-level VI.
Print_IV_curves : Plot the IV curves. This subVI is dynamically linked, unlike the previous.
Print_current_vs_time : Plot the current versus time. It is dynamically linked too.

4.2.4 Single channel controller

The *Single channel controller* was developed to allow access to all parameters of a single channel. It was useful for development purpose, allow us to test all the communication packets and to create special configuration that will never appends with the final programs. It can be useful in the future if someone want to use the SCT HV cards as general purpose power supplies. Figure 45 presents its

graphical user interface.

This application rely mainly on the *Channel_ control* subVI and has been used to develop and test it. This subVI is then always used when something must be read or write from / to the on-card channel micro-controller.

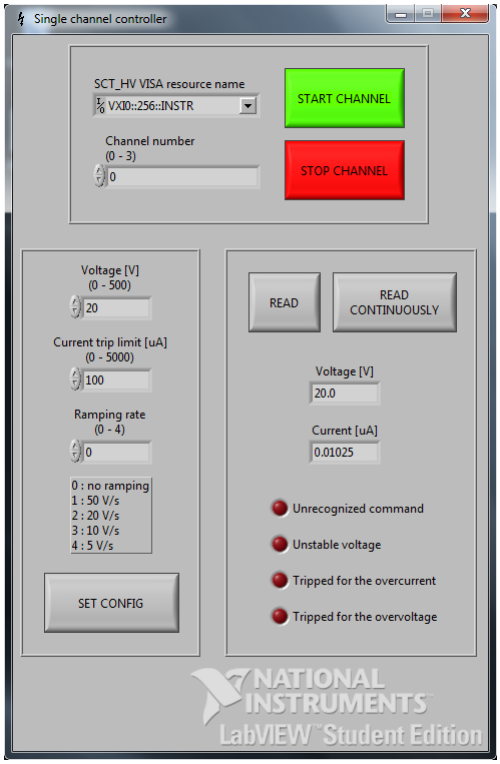


Figure 45: Single channel controller user interface

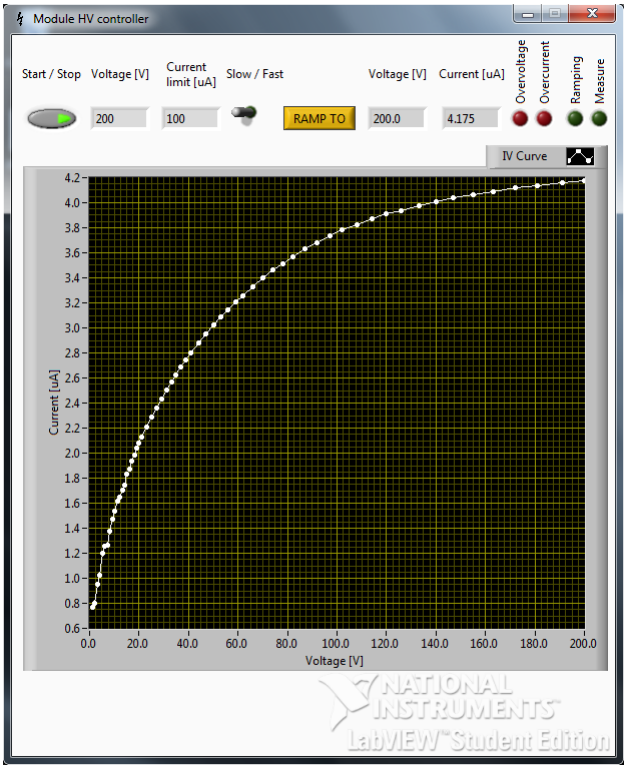


Figure 46: Module HV controller user interface after sensor IV curve measurement

4.2.5 Module HV controller

The *Module HV controller* is designed to allow the high voltage powering of a single Module. It is capable to start and stop the power. You can set the voltage you want to reach and the current limit. The Module will be powered off if this current is exceeded. It can then ramp to the selected voltage from the actual voltage, measuring periodically the voltage and the current. An IV curve will be printed at the end of the ramping. There is two ramping modes : slow and fast. This influence the number of measured points and the ramping speed. It has been added to allow a slow powering up with precise IV curve measurement and a fast powering up when IV curves are not necessary. It is time saving when you perform multiple measurements and power cycles the same day. The voltage and current are numerically printed in realtime. Two Light-Emitting Diodes (LEDs) indicate if an over-voltage or over-current happens. If this is the case, you have to stop and restart manually. Two LEDs indicate if the system is actually ramping or measuring. Figure 46 shows the user interface.

This application was tested on a real sensor to validate its usefulness and measure the noise influence of these PS cards. The measurement results can be found in section 5.2.5. It was then improved and modified to become the *Stavelet HV controller*.

4.2.6 Stavelet HV controller

The goal and features of the *Stavelet HV controller* is mostly identical to the *Module HV controller*. The point is that instead of powering one Module, it need to power eight of them independently and simultaneously. The main user interface is shown on figure 47.

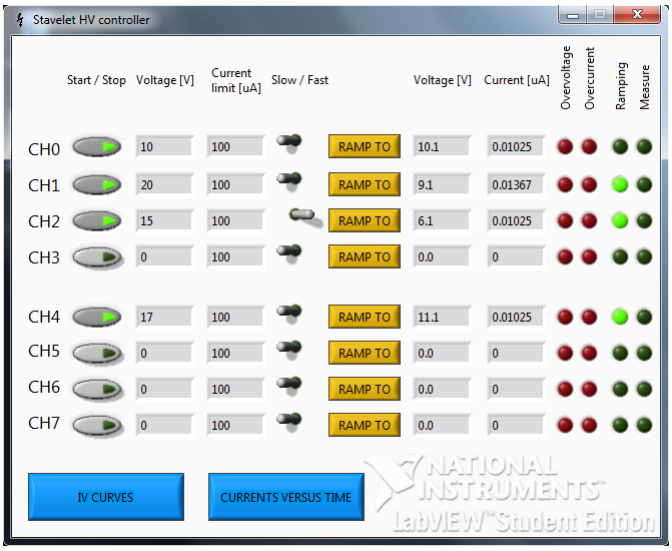


Figure 47: Stavelet HV controller : main user interface

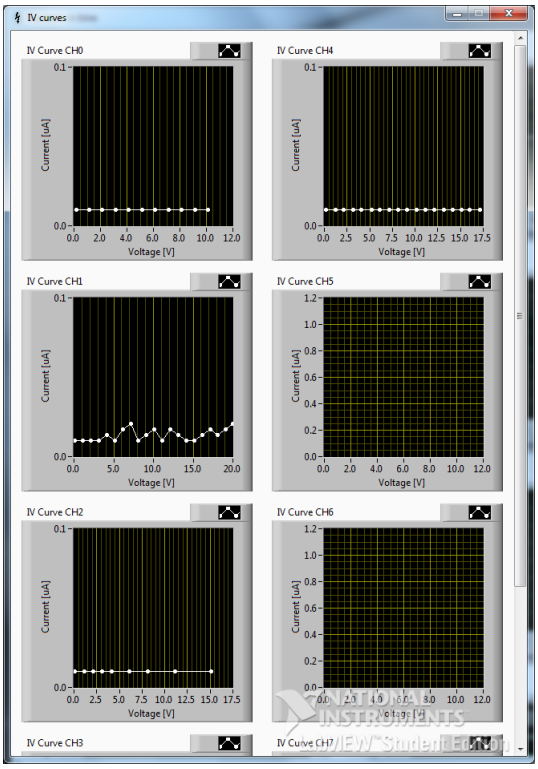


Figure 48: Stavelet HV controller : IV curves window

To keep the main interface clear and intuitive, the IV curves have been moved on a separate window. This allow the user to open or close this window according to his actual needs. The IV curves printed are always the last measured ones, even if the window was closed and reopened. Figure 48 shows this window. The printed IV curves were measured unladen, the Stavelet was not available at this time.

A new feature of the *Stavelet HV controller* is to display the current versus time. This permit us to studied the bias current variation that can happens due to temperature drift. These plots are on a separate window too, figure 49.

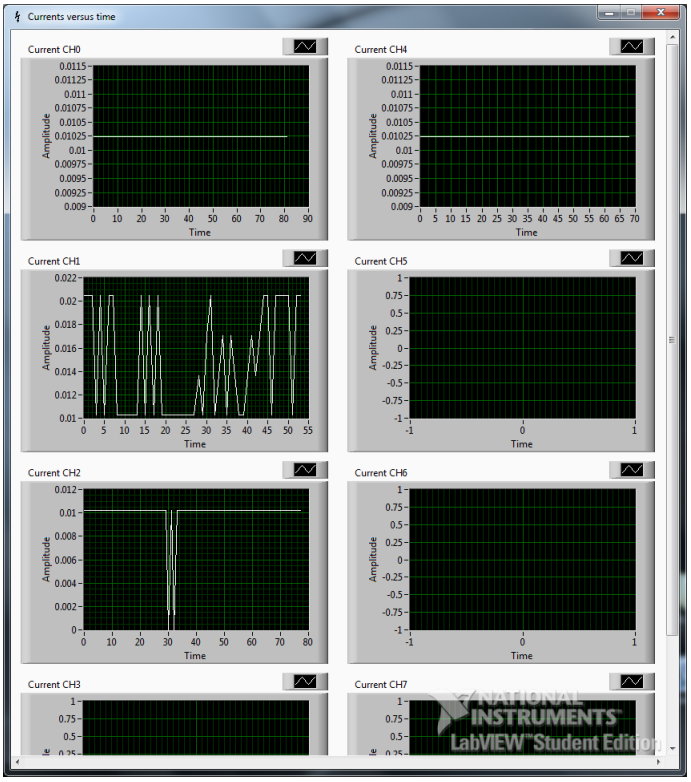
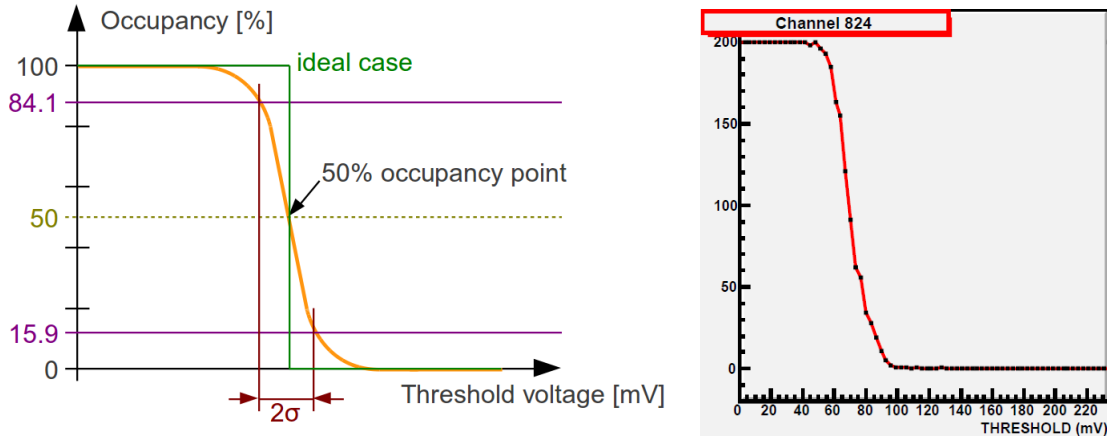


Figure 49: Stavelet HV controller : currents versus time window

4.3 Noise measurements

SCTDAQ is a ROOT based software providing support for Module testing. It communicates with the HSIO for data acquisition and performs data analysis on a PC to extract and display the sensor performance parameters, such as noise or response curves.

To simulate the passage of a charged particle, the readout electronics (described in section 3.2) is able to inject a charge (ten different values from 0.5 to $7fC$) on each of its own channels. A threshold scan is performed on each channel for different injected charge. Namely we set the threshold voltage (digitally controlled) to its lower value, measure the occupancy, increase the threshold voltage, measure again. We do it until the threshold voltage reach its higher value. The occupancy is obtained by calculating the percentage of hits over many readouts, building up a statistical picture of how the channel behaves. The occupancy is then plotted as a function of the threshold, so called an S-curve. As long as the input signal is above the currently set threshold an occupancy of 100% is expected. By increasing the threshold the occupancy of the channels drops to 0 as soon as the input signal is lower than the threshold. Thus this S-curve ideally would have a shape of a step function but in reality is smeared out due to the noise present in the system. An example, measured by SCTDAQ on an ABCN channel, is shown on figure 50(b). Figure 50(a) shows the parameters : the 50% occupancy point and the standard deviation σ. The green curve represents the ideal case where a selected charge would always produce the same pulse.



(a) Parameters definition (b) Measured by SCTDAQ

Figure 50: S-curve

The 50% occupancy point is defined by the threshold voltage for which half the readouts are hits. It is the most probable pulse amplitude for a given injected charge, the estimated response. Figure 51 shows a response curve, a plot of the estimated response versus the injected charge. By deriving a second-order polynomial fit of the response curve, we obtain the small signal gain. An example calculated by SCTDAQ on an entire ABCN (averaging of its 128 channels) is shown on figure 52(b).

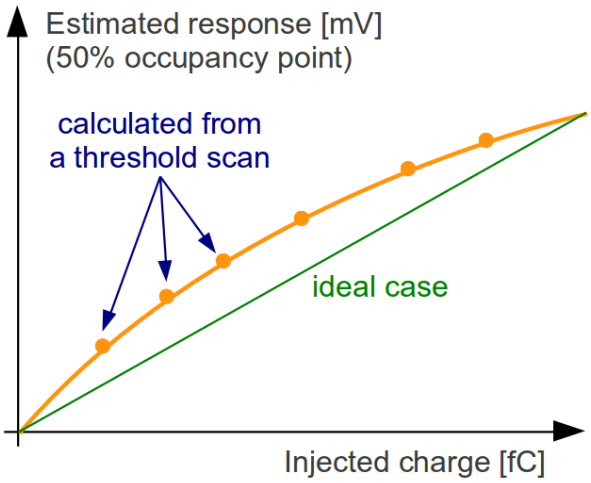
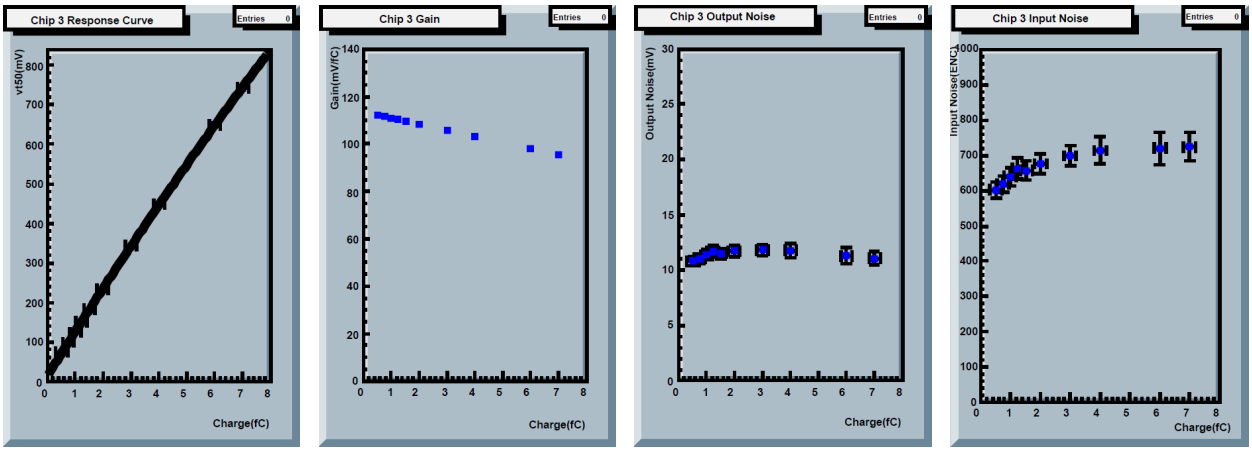


Figure 51: Response curve of a channel

2σ is defined by the delta between the threshold voltage for which 84.1% and 15.9% of the readouts are hits. The standard deviation σ represents the output noise, after the analog readout electronics. A plot of the output noise versus the injected charge, measured by SCTDAQ, is shown on figure 52(c).

The input noise is obtained by dividing the output noise by the small signal gain for each injected charge. The elementary charge being $1.602176487 \cdot 10^{-19} C$, we can state the input noise in Equivalent Noise Charge (ENC). A plot of the input noise versus the injected charge, measured by SCTDAQ, is shown on figure 52(d).



(a) Response curve (b) Small signal gain (c) Output noise (d) Input noise

Figure 52: SCTDAQ measurements on an ABCN chip

Instead of printing the input noise as a function of the injected charge, we can plot its value for each channel at a selected injected charge. Figure 53 shows an example generated by SCTDAQ over 1280 channels, namely a column of strips.

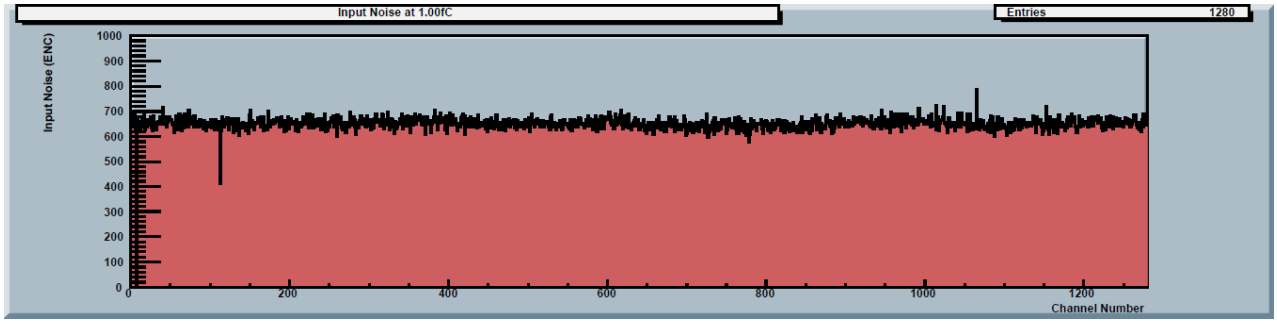


Figure 53: Input noise over 1280 channels, one sensor row, printed by SCTDAQ

5 Electrical measurements

The noise measurements done during this thesis are presented in this chapter. All the measures were performed with water cooling at 6° using the "3PointGain at 1fC" SCTDAQ test. This test performs a threshold scan (from 0 to 233.6mV in 3.2mv steps) at three different charges (0.5, 1 and 1.5fC) on each channel (5120 per Module) and extracts the input noise at 1fC in ENC. See section 4.3 for the noise extraction method. The noise values are average noise over entire columns of 1280 channels each. Sometimes over entire Hybrids (two columns, 2560 channels). See figures 8 and 11 for columns and Hybrids physical positions. Hybrid 61 handles columns 0 and 1, Hybrid 62 columns 2 and 3.

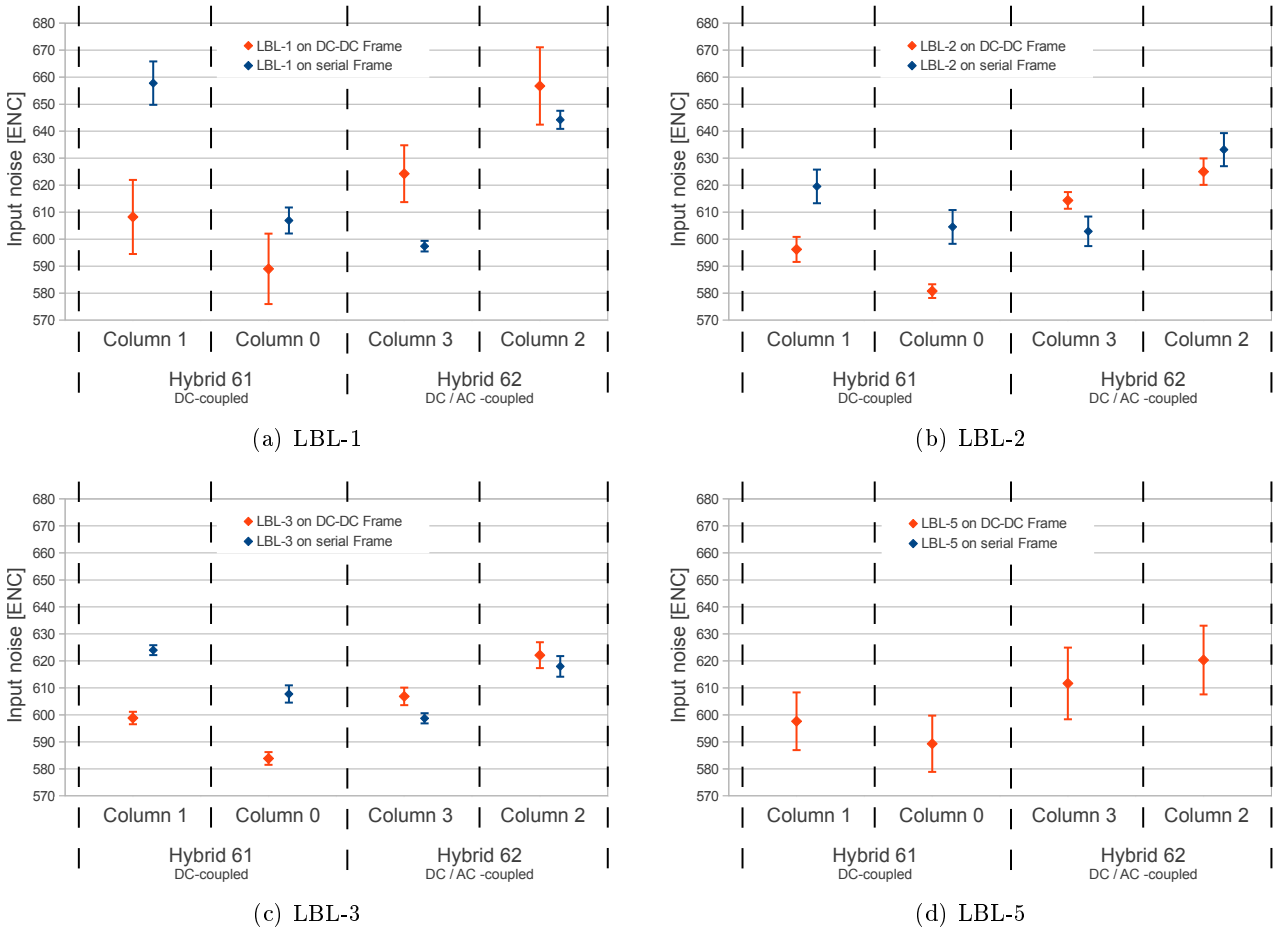
We will first present the characterization of each single Module, before its installation on the Stavelet. We will then compare the Module and the Stavelet test setups with respect to the noise influence to assure that the further Stavelet noise values measured with the Stavelet test setup will be comparable with the previous Modules characterization done with the Module test setup. We will finally compare the Modules before and after their installation on the Stavelet Core.

5.1 Characterization of individual Modules before installation on the Stavelet

We need to characterize every single Module before its installation on the Stavelet Core to be able to compare their performances and study if the Stavelet has any influence and which. These noise values are called baseline noise.

Due to the DC-DC powering scheme on the first assembled side of the Stavelet, we need to characterize the Modules on the DC-DC Frame. The four Modules have been transferred on this Frame for these measurements.

The tricky thing is the statistical distribution of the measurements. We need several measurements to build a representative dataset, then extract the mean value and the standard deviation. Figures 54 compare the Modules input noise with respect to the powering scheme.



(a) LBL-1

(b) LBL-2

(c) LBL-3

(d) LBL-5

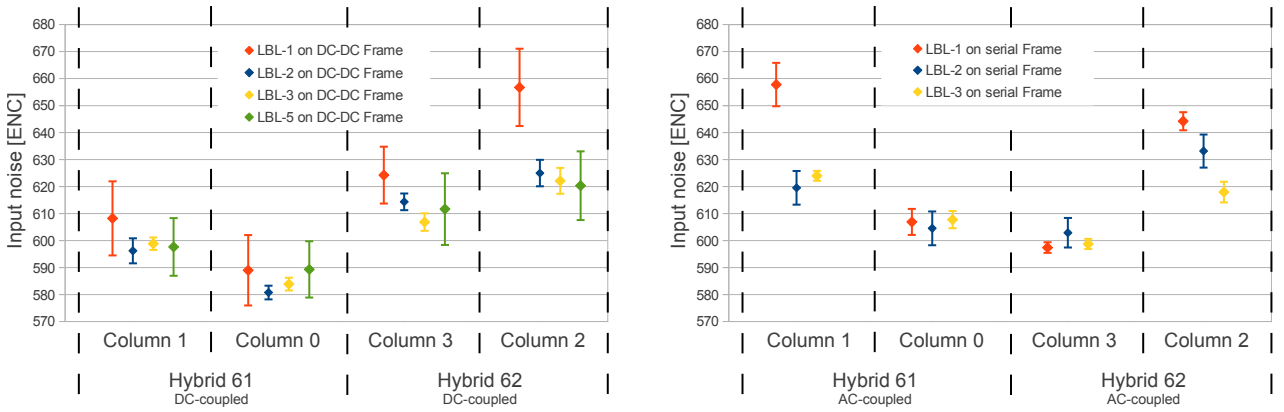
Figure 54: Input noise analysis

There is no measurements of the LBL-5 on a serial Frame simply because it was never mounted on it. LBL-4 is missing : it exists but won't be installed on the Stavelet because one of its ABCN is damaged.

First observation : column 1 is noisier than column 0, column 2 than column 3. The noise is lower on the center columns because they are more "shielded" from the outside (noisy) environment if they are in the center. This is particularly important for the individual Module test setup. And it has been observed by the other groups of the collaboration.

Second observation : DC-coupled Hybrid 61 is noisier when it is serially powered. There is no significant difference on Hybrid 62, at least for LBL-2 and LBL-3. Hybrid 62 is AC-coupled on a serial Frame and DC-coupled on a DC-DC Frame.

Another interesting plot is an input noise comparison between the Modules using the same powering scheme. Such a plot is shown on figure 55(a) for the DC-DC powering scheme and on figure 55(b) for the serial powering one.



(a) DC-DC (b) Serial

Figure 55: Modules noise comparison

Figures 55 show that the noise level is constant across the Modules. This means that the Modules's characteristics are stable. Noise is higher on Module LBL-1 because the glue layer from sensor to Hybrids is thinner, since the process was not completely controlled yet.

The input noise values of the four Modules that will be installed on the Stavelet DC-DC side is summarized in table 2.

Module	Powering	Hybrid 61 Column 0	Hybrid 61 Column 1	Hybrid 61 Columns 0&1	Hybrid 62 Column 2	Hybrid 62 Column 3	Hybrid 62 Columns 2&3
LBL-1	serial	607	658	**621**	644	597	**632**
LBL-1	DC-DC	589	608	**599**	657	624	**641**
LBL-2	serial	605	620	**612**	633	603	**618**
LBL-2	DC-DC	581	596	**589**	625	614	**620**
LBL-3	serial	608	624	**616**	618	599	**608**
LBL-3	DC-DC	584	599	**591**	622	607	**615**
LBL-5	serial	-	-	-	-	-	-
LBL-5	DC-DC	589	598	**594**	620	612	**616**

the values are the mean noise over all channels of a column or an Hybrid
all values are given as ENC (elementary charge e^-)

Table 2: Baseline noise of each Module that will be installed on the Stavelet DC-DC side, with respect to the powering scheme.

5.2 Comparison of noise influence between Module and Stavelet test setups

To be able to test the Stavelet, we have built a new test setup. We want to keep the Module test setup because we'll need to test Modules in parallel as well. So we have to duplicate the material needed for the tests : power supplies, HSIO board, PC, software and test box. Of course we want to know the noise influence of each individual addition to be able to perform reliable comparison on Modules before and after their installation on the Stavelet Core. So we have tested each duplicate material separately.

Almost all the comparisons have been done with a DC-DC and a serially powered Module. The serially powered Modules are always more sensitive to noise, this as been observed many times. We will see

this on these comparisons too. The selected serially powered Module is the LBL-2, best ever built here and attempted to be the most sensitive to noise. The DC-DC powered Module will be the LBL-3, thePS only one available at this time. In preparation of the Stavelet assembly (DC-DC side first), the Modules are progressively transferred to the DC-DC Frame for characterization. Some tests have then been done with the LBL-2 on the DC-DC Frame or without serially powered Module (LBL-2 was the last one).

5.2.1 HSIO powering scheme

Before comparing HSIO boards or power supplies, we need to analyse the powering scheme influence and choose one to perform further comparisons.

This board is normally supplied with $48V$ and an internal DC-DC convert it down to $12V$. Nothing on the card uses the $48V$. The only goal of this design is to reduce power loss over long line due to higher current.

We can also power the board directly with $12V$. We've already noticed noise differences (especially with serially powered Modules) depending on the powering mode. We want to confirm this and verify that it was not a problem of our old HSIO. So all the comparisons are done with the two HSIOs.

The tables 3 and 4 show the results with a DC-DC and a serially powered Module, respectively. The column 1 corresponds to the Hybrid 61 column 1, column 2 to Hybrid 61 column 2, column 3 to Hybrid 62 column 1, column 4 to Hybrid 62 column 2.

HSIO SLAC ID	**Powering scheme**	**Hybrid 61 Column 0**	**Hybrid 61 Column 1**	**Hybrid 62 Column 2**	**Hybrid 62 Column 3**
18019831 (glsModule)	$48V$	592	608	646	624
18019831 (glsModule)	$12V$	582	598	620	604
18022642 (glsStavelet)	$48V$	585	599	626	610
18022642 (glsStavelet)	$12V$	582	596	623	609

the values are the mean noise over all channels of a column
all values are given as ENC (elementary charge e^-)

Table 3: HSIO powering scheme comparison, noise values measured on the DC-DC powered LBL-3 Module

HSIO SLAC ID	**Powering scheme**	**Hybrid 61 Column 0**	**Hybrid 61 Column 1**	**Hybrid 62 Column 2**	**Hybrid 62 Column 3**
18019831 (glsModule)	$48V$	685	705	749	715
18019831 (glsModule)	$12V$	604	615	629	598
18022642 (glsStavelet)	$48V$	620	628	637	614
18022642 (glsStavelet)	$12V$	604	612	627	599

the values are the mean noise over all channels of a column
all values are given as ENC (elementary charge e^-)

Table 4: HSIO powering scheme comparison, noise values measured on the serially powered LBL-2 Module

The noise created by the internal DC-DC converter (when powered with $48V$) is confirmed with the two powering schemes : DC-DC and serial.

When powered in $48V$, the new HSIO appears to be less noisy, especially when the Module is serially powered. We'll continue to power them in $12V$ anyway.

5.2.2 HSIO boards

We now test the newly received (from UK) HSIO board (SLAC ID 18022642). We have performed some tests to verify its conformity and noise influence.

As previously discussed, we power them with $12V$ for comparison and testing.

The tables 5 and 6 show the results with a DC-DC and a serially powered Module, respectively.

HSIO SLAC ID	**Hybrid 61 Column 0**	**Hybrid 61 Column 1**	**Hybrid 62 Column 2**	**Hybrid 62 Column 3**
18019831 (glsModule)	582	598	620	604
18022642 (glsStavelet)	582	596	623	609

the values are the mean noise over all channels of a column
all values are given as ENC (elementary charge e^-)

Table 5: HSIO boards comparison, noise values measured on the DC-DC powered LBL-3 Module

HSIO SLAC ID	**Hybrid 61 Column 0**	**Hybrid 61 Column 1**	**Hybrid 62 Column 2**	**Hybrid 62 Column 3**
18019831 (glsModule)	604	615	629	598
18022642 (glsStavelet)	604	612	627	599

the values are the mean noise over all channels of a column
all values are given as ENC (elementary charge e^-)

Table 6: HSIO boards comparison, noise values measured on the serially powered LBL-2 Module

We can conclude that there is no significant differences between the two HSIO boards when powered in $12V$.

5.2.3 HSIO 12V power supplies

As previously said, we'll power the HSIO board with $12V$ for priceless lower noise. We'll compare the noise influence between different power supplies. The HSIO used for this comparison is the SLAC ID 18019831 (old).

The tables 7 and 8 show the results with a DC-DC and a serially powered Module, respectively.

HSIO PS	**Hybrid 61 Column 0**	**Hybrid 61 Column 1**	**Hybrid 62 Column 2**	**Hybrid 62 Column 3**
HP E3610A (glsModule)	579	591	623	611
pd TP340A (glsStavelet)	580	597	627	617

the values are the mean noise over all channels of a column
all values are given as ENC (elementary charge e^-)

Table 7: HSIO $12V$ power supplies comparison, noise values measured on the DC-DC powered LBL-2 Module

HSIO PS	**Hybrid 61 Column 0**	**Hybrid 61 Column 1**	**Hybrid 62 Column 2**	**Hybrid 62 Column 3**
HP E3610A (glsModule)	599	616	626	599
pd TP340A (glsStavelet)	599	620	634	603

the values are the mean noise over all channels of a column
all values are given as ENC (elementary charge e^-)

Table 8: HSIO $12V$ power supplies comparison, noise values measured on the serially powered LBL-2 Module

Since there is no significant difference, this test was not performed on a DC-DC powered Module that will be even less sensitive.

5.2.4 LV power supplies

We have bought a new two channels PS (Sorensen XPF 60-20DP), capable to power both the DC-DC and and the serial sides of the Stavelet at the same time. We want to see if there is some noise differences with the previously used PS (Lambda GENH150-5).

The tables 9 and 10 show the results with a DC-DC and a serially powered Module, respectively.

LV PS	**Hybrid 61 Column 0**	**Hybrid 61 Column 1**	**Hybrid 62 Column 2**	**Hybrid 62 Column 3**
LAMBDA GENH150-5 (glsModule)	587	601	618	606
Sorensen XPF 60-20DP (glsStavelet)	582	598	618	603

the values are the mean noise over all channels of a column
all values are given as ENC (elementary charge e^-)

Table 9: LV power supplies comparison, noise values measured on the DC-DC powered LBL-3 Module

LV PS	Hybrid 61 Column 0	Hybrid 61 Column 1	Hybrid 62 Column 2	Hybrid 62 Column 3
HP 6541A (glsModule)	597	615	634	603
Sorensen XPF 60-20DP (glsStavelet)	611	623	642	606

the values are the mean noise over all channels of a column
all values are given as ENC (elementary charge e^-)

Table 10: LV power supplies comparison, noise values measured on the serially powered LBL-2 Module

There is no significant difference in the case of DC-DC powering. However there is more noise ($8.25e^-$ on average) in the case of serial powering. We will have to characterize the serially powered Modules with this new PS before their installation on the second side of the Stavelet. This work is not part of this thesis, the second side will be assembled later.

5.2.5 HV power supplies

As already explained in section 4.2, we need an eight channels HV PS. We want to measure its noise influence compared to the actual source (Keithley 2410 1100V SourceMeter).

The table 11 and 12 show the results with a DC-DC and a serially powered Module, respectively.

HV PS	Hybrid 61 Column 0	Hybrid 61 Column 1	Hybrid 62 Column 2	Hybrid 62 Column 3
Keithley 2410 (glsModule)	579	591	623	611
SCT HV card 1 CH0 (glsStavelet)	579	591	623	614
SCT HV card 2 CH3 (glsStavelet)	578	592	629	616

the values are the mean noise over all channels of a column
all values are given as ENC (elementary charge e^-)

Table 11: HV power supplies comparison, noise values measured on the DC-DC powered LBL-2 Module

HV PS	Hybrid 61 Column 0	Hybrid 61 Column 1	Hybrid 62 Column 2	Hybrid 62 Column 3
Keithley 2410 (glsModule)	605	624	623	595
SCT HV card 1 CH0 (glsStavelet)	618	631	636	615
SCT HV card 2 CH3 (glsStavelet)	605	624	638	603

the values are the mean noise over all channels of a column
all values are given as ENC (elementary charge e^-)

Table 12: HV power supplies comparison, noise values measured on the serially powered LBL-2 Module

There is some differences with the serially powered Module. This is probably due to the longer cable used. A second measure with a DC-DC Module will be done to confirm or infirm this result.

5.2.6 Software installations

SCTDAQ software and the firmware (HSIO Virtex 4 FPGA configuration) are continuously under development in the UK. They use their Stavelet to perform tests before the release of a new stable version. *ROOT*[6], used by *SCTDAQ*, is under development too. We've installed the last software versions on the PC and used the last firmware for the Stavelet test setup. Because there is bugs correction between versions, we want to compare them to see if there is any noise value difference.

The table 13 shows the results with a DC-DC powered Module.

SCTDAQ version	**Hybrid 61 Column 0**	**Hybrid 61 Column 1**	**Hybrid 62 Column 2**	**Hybrid 62 Column 3**
Old PC (glsModule)	578	594	618	608
New PC (glsStavelet)	582	596	628	617

the values are the mean noise over all channels of a column
all values are given as ENC (elementary charge e^-)

Table 13: software installations comparison, noise values measured on the DC-DC powered LBL-2 Module

There is no significant noise difference between the two software installations.

5.2.7 Complete test setups

After comparisons of individual components, we can now compare the entire setups. This contain different computer, software and firmware versions, power supplies and HSIO board.

The table 14 shows the results with a DC-DC powered Module.

Test setup	**Hybrid 61 Column 0**	**Hybrid 61 Column 1**	**Hybrid 62 Column 2**	**Hybrid 62 Column 3**
Module	583	602	630	618
Stavelet	584	601	628	615

the values are the mean noise over all channels of a column
all values are given as ENC (elementary charge e^-)

Table 14: Complete test setups comparison, noise values measured on the serially powered LBL-2 Module

There is absolutely no noise influence difference between the Module and the Stavelet test setups.

5.2.8 Conclusion

We can conclude that the noise levels measured during the characterization of each Module on the Module test setup is comparable to the noise levels measured on the Stavelet with the Stavelet test

[6] the framework developed at CERN to handle and analyse large amounts of data, see `root.cern.ch`

setup, at least for the DC-DC powered side. Further measurements are needed for the serially powered side. Anyway the Modules composing it are not yet assembled.

5.3 Noise comparisons between individual Modules and Stavelet

As described in chapter 3, we have two Modules on the Stavelet DC-DC side. The LBL-5 was damaged during its transfer from the DC-DC Frame to the Stavelet. We have only one Module to test against input noise level, the LBL-3. Figure 56 shows the results. All the columns are noisier, especially on Hybrid 61. Further measurements and analysis have to be down to identify the source of this additional noise.

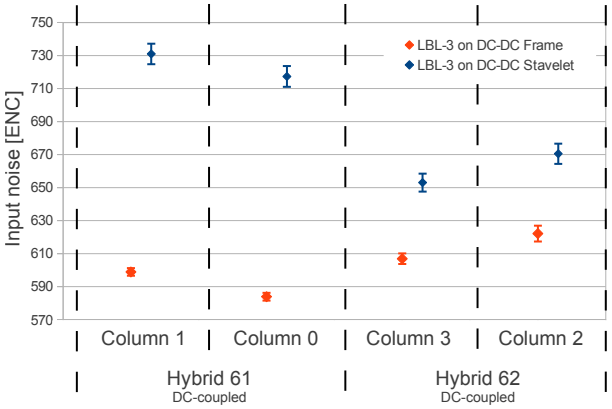


Figure 56: LBL-3 noise analysis

6 Conclusion

This project, divided into three parts, was multi-disciplinary. It included the development of mechanical tools, mechanical assembly, metrology measurements, software development, noise studies etc. We will conclude on each part separately.

6.1 Stavelet assembly

The US Stavelet was partially assembled during this thesis. All the steps for the Stavelet mounting were completed. Two Modules are missing on the DC-DC side due to delays at the different stages of the project. The silicon sensor of the Module LBL-5 was damaged, but the electronics works fine. The second installed Module LBL-3 works fine.

6.2 Test systems

A new test setup was installed during this project to test the Stavelet. We had already a Module test setup and wanted to keep it to continue Module testing in parallel of Stavelet testing. This work includes a lot of varied tasks : plumbing for water cooling, nitrogen pipes, PC installation, software deployment, mechanical assembly etc.

Three SCT HV controllers have been developed : the single channel controller, the Module HV controller and the Stavelet HV controller. The last two have been used for Modules and Stavelet testing, controlling and monitoring the sensors bias voltage. Theses programs were the occasion for me to learn and start using LabVIEW. I became familiar with the dataflow programming paradigm, multi-threading, inter-thread communication, multi-windows program and applications builder.

6.3 Electrical measurements

All the Modules were characterized with respect to the noise before their installation on the Stavelet. These results show a constant noise level across Modules and are consistent with the ones of the other groups.

The new built Stavelet test setup was characterized with respect to the noise influence of each of its individual component. The results show that the noise measurements obtained with the Stavelet test setup are comparable to the ones obtained with the Module test setup.

Finally the Modules were measured when installed on the Stavelet. LBL-5, being damaged, was not measured against noise, but it is still useful for communication tests. LBL-3 was successfully measured. This happening the very last day, time was missing for further analysis and improvements.

6.4 Further perspectives

This Stavelet will provide the LBNL with an up-to-date Stave prototype, allowing the LBNL ATLAS collaboration to test their embedded bus tape and compare the results with the baseline Stavelet

prototypes. It will allow them to study the noise influence between face-to-face Modules, one on each side of the Core. The confirmation or invalidation of the previous observations and conclusions is also possible, notably with respect to the powering schemes. New shielding and grounding configurations may show different results too. Another long-term goal is to keep the know-how and to prepare the mass production. A large amount of Modules (20'000) and Staves (1000) will be produced around the world. LBNL will participate in the effort.

6.5 Personal experience

It was a great experience for me to be at LBNL for three months working on the ATLAS experiment. I have learned a lot about particle physics and how particle detectors work, especially silicon trackers. It was interesting to deal with high technologies and see how the development of a large and long-term experiment is internationally managed, split into several groups.

References

[CER11] CERN. *SCTUpDAQDown.* `https://twiki.cern.ch/twiki/bin/viewauth/Atlas/SCTUpDAQDown`, July 2011.

[CVG02] Jean-Claude Clemens, Eric Vigeolas, and Claudia Gemme. *Module cooling support adhesives.* June 2002.

[Leh11] Niklaus Lehmann. *Characterization of the Large Hadron Collider Sensor Array Modules.* École d'ingénieurs et d'Arichtectes de Fribourg, August 2011.

[LW10] on behalf of the ATLAS Collaboration Liv Wiik. *ATLAS Tracker Upgrade: Silicon Strip Detectors for the sLHC.* Physikalisches Institut, Albert-Ludwigs-Universität Freiburg, July 2010.

[MC12] on behalf of the ATLAS Collaboration M. Cobal. *ATLAS Upgrades Towards the High Luminosity LHC.* INFN and University Udine, July 2012.

[SCT04] *SCT HV, VME Model HV203, User Manual.* Institute of nuclear physics, ATLAS experiment laboratory, Krakow, Poland, 2004.

[SDC11] on behalf of the ATLAS Upgrade strip tracker Collaboration Sergio Díez Cornell. *Silicon strip staves and petals for the ATLAS Upgrade tracker of the HL-LHC.* December 2011.

[Spi05] Helmuth Spieler. *Semiconductor Detector Systems.* Oxford Science Publications, 2005.

A Module test procedure

A.1 Prepare for testing

We have to perform the following steps to start up the Module. Then we can do the tests we want.

The purpose of this guide is not to be a formal procedure with full explanation. It's just a memo to help us during Module testing.

These steps include some SCTDAQ tests. For information about what they do and why, see section 4.3 about noise measurements or SCTDAQ documentation. [CER11]

1. Disassemble the module from his storage box.
2. Turn on the vacuum to maintain the module into the test box.
3. Put the module into the test box
4. Tighten the screw that makes the HV ground connection.
5. Plug in all the connectors. Don't forget the ground of the box and the NTC.
6. Close the test box.
7. Test the HV connection :
   - Set to $-1V$.
   - The current should be about $2\mu A$.
   - Open the box.
   - The current should be about $100\mu A$ (current limited) due to light.
   - Close the box.
   - Set it back to $0V$.
8. Start the cooling (set it to $6°C$).
9. Start the nitrogen to avoid moisture.
10. Put the black tissue on the box to avoid lighting.
11. Power on the buffer module (2x Recall). Settings : $4.5V$ and $2.5A$.
12. Power on the HSIO board. Settings : $12V$ and $1.6A$.
13. Substitute the D disk : subst D: C:\sctdaq
14. Configure the FPGA :
    - Start *iMPACT*.
    - Don't open or create a project.
    - Double click on Boundary Scan.
    - Right click : Initialize Chain.
    - Select two times the file name D:\Firmware_files\hsio_c01_eos_top_v310d_16histo.
    - Say OK to the programming properties.
    - Right click on the FPGA (xc4vfx60): Program then OK.
    - Eventually (if we want to restart the HSIO board without FPGA reconfiguration) program the EEPROM (xcf32p): Right click and Program.
    - Close *iMPACT*. Don't save the project.
15. Wait for the module to be cold (check the NTC, $13k\Omega$ corresponds to $20°C$). Will be around $21k\Omega$ when module is idle and $15k\Omega$ when module is in operation.
16. Power on the HV slowly to $-10V$.
17. Power on the LV :
    - If DC/DC powering : attach the alligator clips and power up the *LAMBDA* power supply (PREV then OUT). The settings are $10.5V$ and $3A$.
    - If serial powering : plug the connectors and power up slowly the *HP* power supply from 0

to $5A$. The voltage will be less than $6V$.
18. Power the HV slowly to his final value : $-200V$. Current will be between 3 and $12\mu A$.
19. Start the *ROOT* software.
20. Start *SCTDAQ* by executing .x Stavelet.cpp.
21. Capture –> Startup BCC V2 (IDC) : check 32,64 / 32,64 to be sure the startup script has been correctly executed.
22. Capture –> Capture BCC ID : check the IDs are 62 and 61.
23. Test –> StrobeDelay(0.25) : set the delay for each ABCN chip.

A.2 Testing

A.2.1 Average noise level

Test –> 3PointGain @ 1fC

Results are in D:\sctvar. The ps folder contains the graphs and the results folder the raw data. The results can be reported in C:\Module testing\Modules\ to keep trace of each module and to do some comparison and analyse.

A.2.2 Channel trim threshold adjustment

Test –> TrimRange

Take approximately 20 minutes to complete. It will set the trim settings. We can then test the module again.

A.2.3 Double trigger

The TrimRange has to be done before this test because he uses the results. Due to some bugs in the software, nothing else can be done after this test. *ROOT* has to be restarted.

To load the sources type .L ABCN_doubleT.cpp in the *ROOT* console. Then execute the test : ABCN_doubleTrio().

A.3 After testing

1. Close the *ROOT* software.
2. Power down the HV slowly to $-10V$.
3. Power down the LV.
4. Power down the HV.
5. Power down the HSIO board.
6. Power down the buffer module.
7. Stop the nitrogen and the cooling.
8. Wait for the module to be at $20°C$. NTC will be around $13k\Omega$.
9. Open the box.

10. Remove all the connectors.
11. Remove the screw.
12. Stop the vacuum.
13. Remove the module.
14. Place it back in his storage box.

B SCT HV controllers user manual

The SCT HV controllers are three LabVIEW programs developed during this thesis. Their description can be found in section 4.2. This user manual describe the installation of the SCT HV cards and the operation of the single channel controller. The Module HV controller and the Stavelet HV controller are very simple to use and do not need a user manual.

B.1 Installation of the cards

There is some steps to perform before we can have access to the VMEbus from the PC.

1. We first need a crate. Then we install the VME controller (by the way the link with the PC) in slot 0. This controller is the NI VME-MXI-2 card. We put our SCT HV cards in other free slots. The crate can be seen on figure 57.
2. We need to install the drivers and the interface software : NI-VXI and NI-VISA. These can be downloaded from *www.ni.com/drivers/*. One will include the other, take the most recent.
3. Power up the crate.
4. Scan the resources with the *Resman* utility : National Instruments –> VXI –> Resman
5. See the result : National Instruments –> VISA –> VISA Interactive Control. We can see the two NI cards (PCI-MXI-2 and VME-MXI-2) on figure 58.

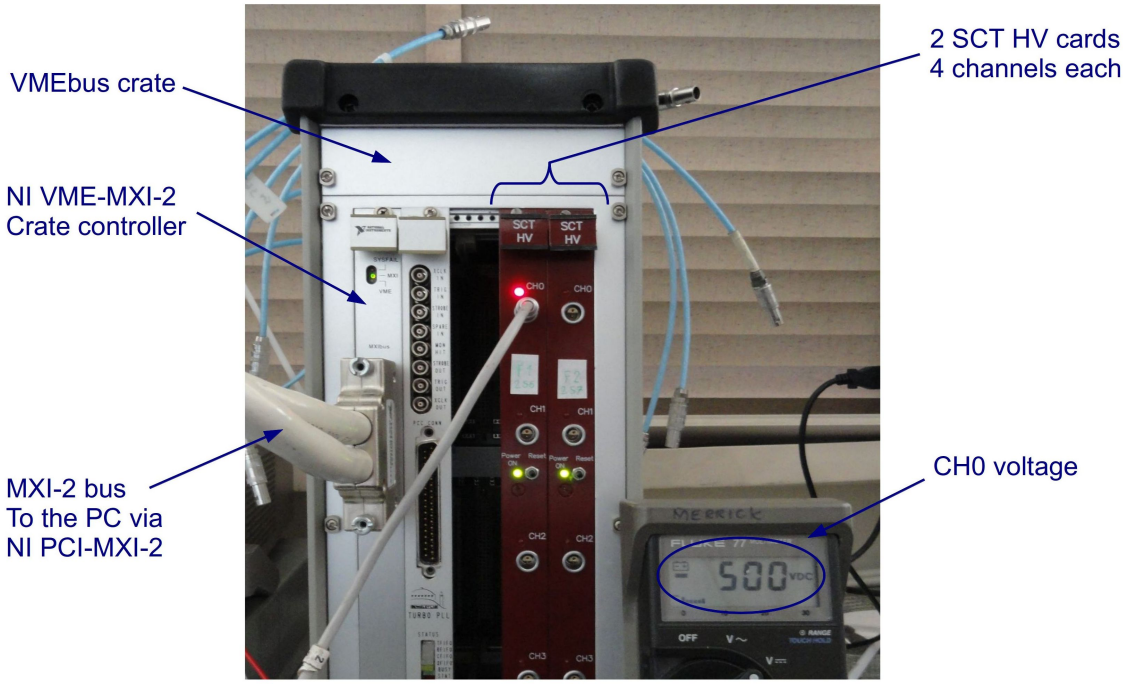


Figure 57: VMEbus crate with NI and SCT HV cards

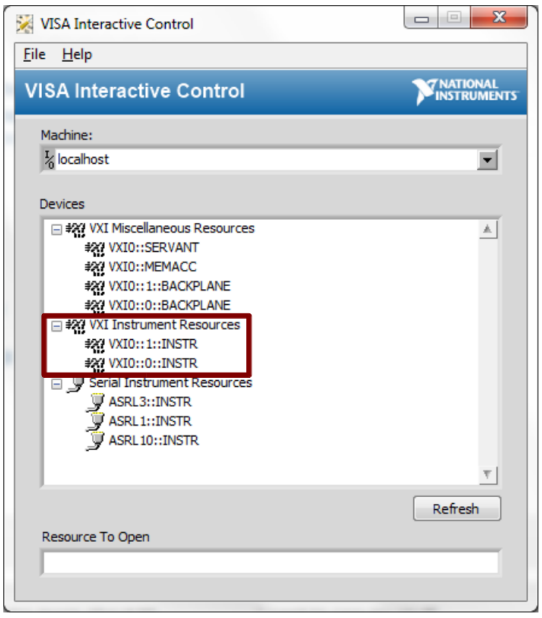


Figure 58: NI cards in VISA interactive control

Now the hardware and software from NI is ready to work.

We must add a VME device for each of our card in the *Measurement & Automation Explorer* (called *MAX*) to gain the access from LabView.

Open the *MAX*, browse the devices tree up to Frame 1 and add to it two VME cards. The devices tree and the first card configuration can be shown on figure 59.

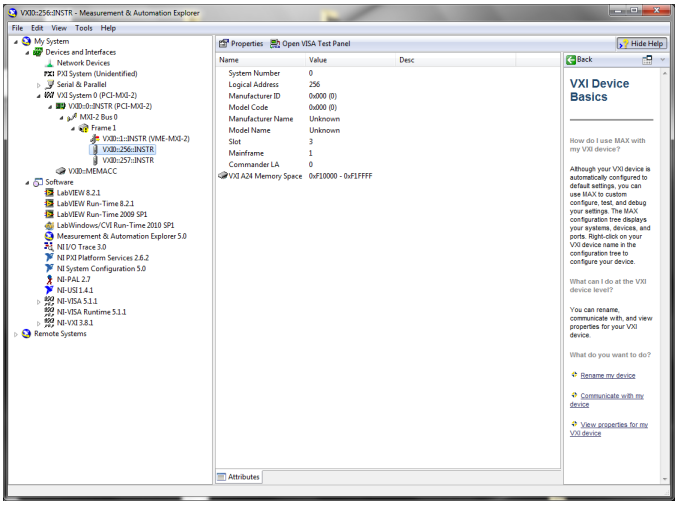


Figure 59: MAX devices tree with SCT HV 1 configuration

The second card configuration can be seen on figure 60.

System Number	0
Logical Address	257
Manufacturer ID	0x000 (0)
Model Code	0x000 (0)
Manufacturer Name	Unknown
Model Name	Unknown
Slot	4
Mainframe	1
Commander LA	0
VXI A24 Memory Space	0xF20000 - 0xF2FFFF

Figure 60: SCT HV 2 configuration

The first two hexadecimal digits of the *VXI A24 Memory Space* is the card physical address. This can be configured by a DIP switch on the card itself. See [SCT04] for more information.

B.2 Single channel controller

This controller is intended to be used like a general power supply. He can set and read all the parameters of a particular channel. The user interface is represented on figure 61

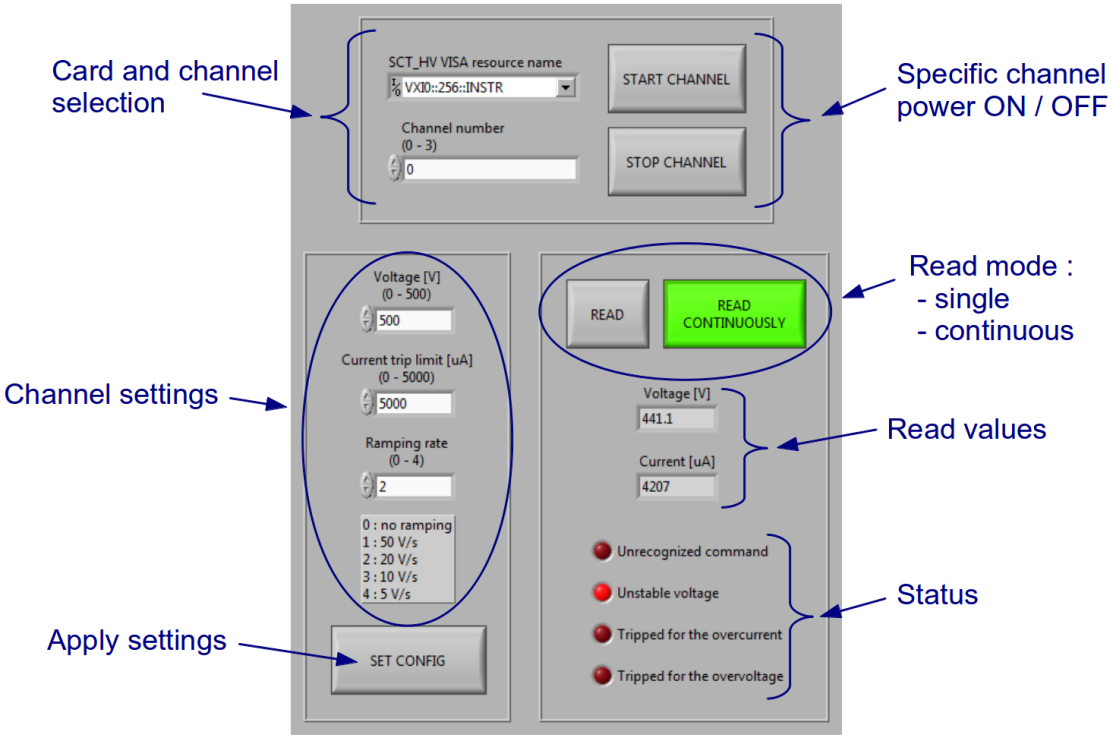


Figure 61: Single channel controller user interface

First we need to select the card we want to use in the drop-down menu. Then we can select one of his four channels. We can then start or stop this channel. If the channel is stopped, the corresponding LED (on the card front panel) is off. If the channel is started, this LED is blinking very slowly (twenty times a minute).

Then we can enter the settings we want to apply. First the voltage we want to reach, from 0 to $500V$. Then the current limit, from 0 to $5000\mu A$. If the current exceed this limit (even during the ramping), the channel will be shut down by the hardware. This is not current limiting. We can also choose one of the four ramping speeds from 5 to $20V/s$, or no ramping at all. When you press the *SET CONFIG* button these settings will be sent to the chosen channel and ramping (up or down) from actual voltage will start.

You can get actual voltage, current and status of the selected channel with the *READ* button. The *READ CONTINUOUSLY* button do the same but every $300ms$ automatically. It's useful to follow a ramping for example.

Status definition :

Unrecognised command : You sent a command that was not comprehensible by the card. This should never appends during normal operation. The program control that the data are valid.
Unstable voltage : This tell you that the channel is actually ramping up or down.
Tripped for overcurrent : The channel has been turned off due to a measured current higher than the current trip limit you specified.
Tripped for overvoltage : The channel has been turned off due to an excessive voltage.

C Stavelet Core raw metrological measurements

These values were measured with a precision optical metrological instrument. They are studied in section 3.7, here only the raw values are mentioned for reference. All the distances are referenced to the mounting reference holes. See figure 21.

N°	x-axis	y-axis	Remark
1	0.0000	0.0000	origin
2	409.7152	0.0000	x-axis alignment
3	409.7391	-130.0747	
4	-0.1358	-130.1026	

all values are given in millimetres

Table 15: Reference holes raw measurements

N°	x-axis	y-axis
1	-87.0469	-129.8313
2	-88.1227	-0.5721
3	412.7267	4.7139
4	413.1348	-136.0413

all values are given in millimetres

Table 16: Edges (x-axis) raw measurements

N°	x-axis	y-axis	Remark
1	-88.0697	9.8279	edge
2	-38.2255	9.8157	
3	12.3268	9.8827	
4	62.6013	9.9368	
5	111.4428	9.9463	
6	162.5699	9.9466	
7	212.5265	9.9686	
8	261.7366	9.9849	
9	312.3788	9.9333	
10	362.5458	9.9293	
11	412.4399	9.8670	edge

all values are given in millimetres

Table 17: Plastic edge raw measurements

N°	x-axis	y-axis	Remark
1	413.0167	-140.0956	edge
2	362.4638	-139.8062	
3	313.4998	-139.8321	
4	262.5586	-139.9856	in the drilled Al
5	212.422	-139.8873	in the drilled Al
6	162.1513	-139.7911	
7	112.1437	-139.7639	
8	61.7901	-139.7017	
9	12.7902	-139.6781	
10	-38.9645	-139.6301	
11	-86.9039	-139.6407	edge

all values are given in millimetres

Table 18: Aluminium edge raw measurements

N°	x-axis	y-axis	Diameter
1	15.0684	-108.0947	3.9950
2	70.5614	-108.1629	3.9959
3	113.1282	-108.1864	3.9943
4	168.5867	-108.2031	3.9976
5	211.1052	-108.2211	3.9916
6	266.5526	-108.1917	3.9984
7	309.0834	-108.1637	3.9907
8	364.5444	-108.1199	3.9956

all values are given in millimetres

Table 19: Bus tape HV contacts raw measurements